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DATA SHEET

PCA5010
Pager baseband controller

Product specification
File under Integrated Circuits, IC17

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Philips
Semiconductors

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1 FEATURES

- Operating temperature range: −10 to +55 °C
- Supply voltage range with on-chip DC/DC converter: 0.9 to 1.6 V
- Low operating and standby current consumption
- On-chip DC/DC converter generates the supply voltage for the PCA5010 and external circuitry from a single cell battery
- Battery low detector
- Low electromagnetic noise emission
- Full static asynchronous 80C51 CPU (8-bit CPU)
- Recovery from lowest power standby Idle mode to full speed operation within microseconds
- 32 kbytes of One-Time Programmable (OTP) memory and 1.25 kbyte of RAM on-chip
- 27 general purpose I/O port lines (4 ports with interrupt possibility)
- 15 different interrupt sources with selectable priority
- 2 standard timer/event counters T0 and T1
- I²C-bus serial port (single 100/400 kHz master transmitter and receiver)
- Subset of standard UART serial port (8-bit and 9-bit transmission at 4800/9600 bits/s)
- 76.8 kHz crystal oscillator reference with digital clock correction for real time and paging protocol
- Real-Time Clock (RTC)
- Receiver and synthesizer control
  - Receiver control by software through general purpose I/Os
  - Synthesizer control by software through general purpose I/Os
  - 6-bit DAC for AFC to the receiver local oscillator
  - Dedicated protocol timer.
- Decoding of paging data
  - POCSAG or APOC phase 1; advanced high speed paging protocols are also supported
  - Supported data rates: 1200, 1600, 2400, 3125 and 3200 symbols/s using a 76.8 kHz crystal oscillator
  - Demodulation of Zero-IF I and Q, 4 or 2 level FSK input or direct data input
  - Noise filtering of data input and symbol clock reconstruction
  - De-interleaving, error checking and correction, sync word detection address recognition, buffering and more is performed by software
  - All user functions (keypad interface, alerter control, display etc.) are implemented in software.
- Musical tone generator for beeper, controlled by the microcontroller
- Watchdog timer
- 48-pin LQFP package.

2 ORDERING INFORMATION

TYPE NUMBER(1)	PRODUCT TYPE	PACKAGE		
		NAME	DESCRIPTION	VERSION
PCA5010H/XXX	pre-programmed OTP	LQFP48	plastic low profile quad flat package; 48 leads; body $7 \times 7 \times 1.4$ mm	SOT313-2

Note

1. Please refer to the Order Entry Form (OEF) for this device for the full type number to use when ordering. This type number will also specify the required program.

3 GENERAL DESCRIPTION

The PCA5010 pager baseband controller is manufactured in an advanced CMOS/OTP technology.

The PCA5010 is an 8-bit microcontroller especially suited for pagers. For this purpose, features such as a 4 or 2 level FSK demodulator, filter, clock recovery, protocol timer, DC/DC converter optimized for small paging systems and RTC are integrated on-chip.

The device is optimized for low power consumption. The PCA5010 has several software selectable modes for power reduction: Idle and Power-down mode of the microcontroller and Standby and OFF mode of the DC/DC converter.

The instruction set of the PCA5010 is based on that of the 80C51. The PCA5010 also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 46 two-byte and 16 three-byte.

This data sheet details the properties of the PCA5010. For details on the I^2C-bus functions see *"The I^2C-bus and how to use it"*. For details on the basic 80C51 properties and features see *"Data Handbook IC20"*.

4 BLOCK DIAGRAM

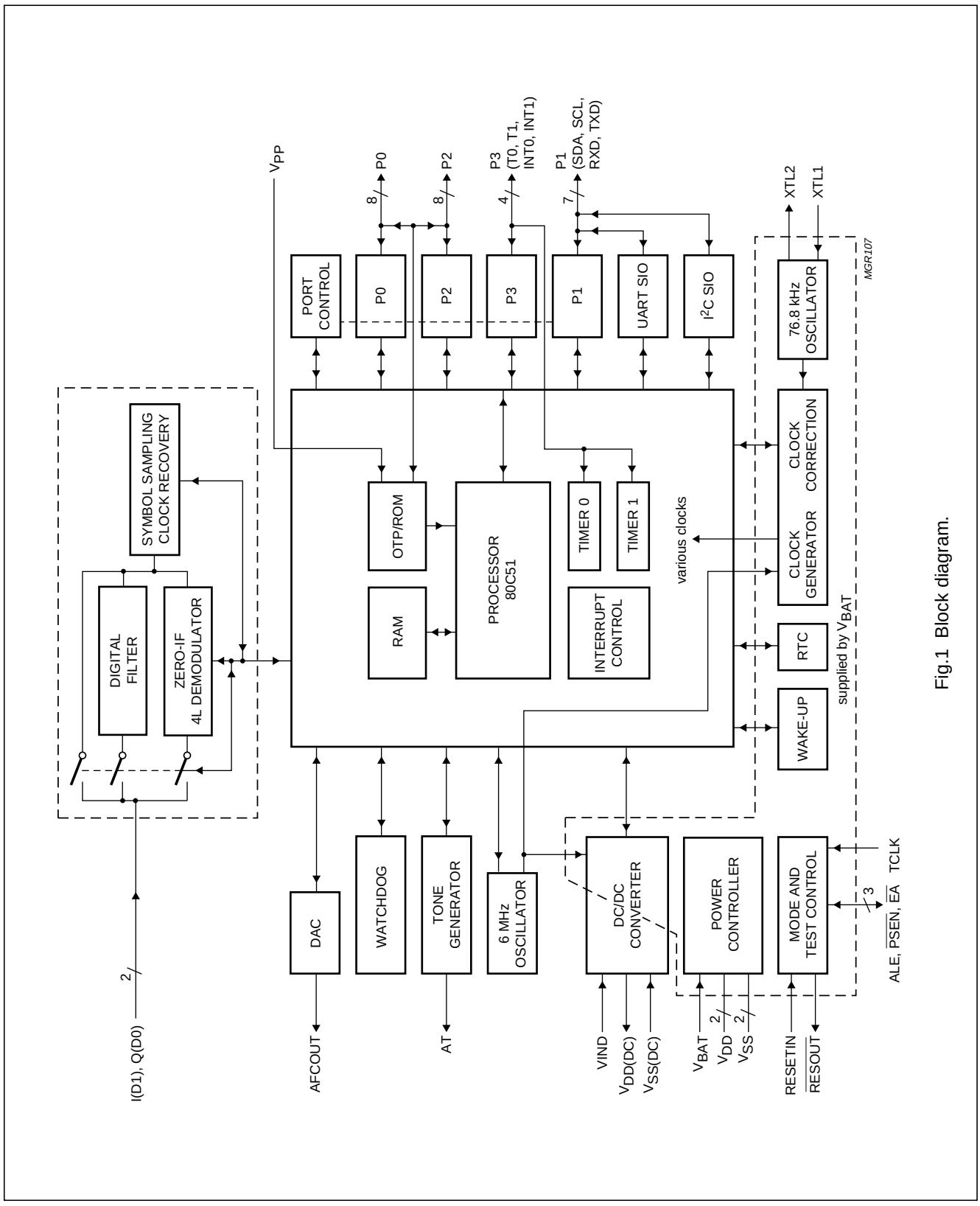


Fig.1 Block diagram.

5 PINNING INFORMATION

SYMBOL	PIN	TYPE	DESCRIPTION
P3.4 and P3.5	1 and 2	I/O	**Port 3:** P3.4 and P3.5 are configured as push-pull outputs only (Option 3R, see Section 6.6). Using the software input commands or the secondary port function is possible by driving the Port 3 output lines accordingly: P3.4 secondary function: T0 (counter input for T0) P3.5 secondary function: T1 (counter input for T1)
AT	3	O	Beeper high volume control output. Used to drive external bipolar transistor.
P2.0 to P2.7	4 to 11	I/O	**Port 2:** Port 2 is an 8-bit bidirectional I/O port with internal pull-ups (option 1S, see Section 6.6.3). As inputs, Port 2 pins that are externally pulled LOW will source current because of the internal pull-ups. (See Chapter 10: I_{pu}). Port 2 emits the high-order address byte during fetches from external program memory. In this application, it uses strong internal pull-ups when emitting logic 1s. Port 2 is also used to control the parallel programming mode of the on-chip OTP.
P0.0 to P0.4	12 to 16	I/O	**Port 0:** Port 0 is a bidirectional I/O port with internal pull-ups (option 1S, see Section 6.6.3). Port 0 pins that have logic 1s written to them are pulled HIGH by the internal pull-ups and can be used as inputs. Port 0 is also the multiplexed low-order address and data bus during access to external program and data memory. In this application, it uses strong internal pull-ups when emitting logic 1s. Port 0 also outputs the code bytes during OTP programming verification.
V_{DDA}	17	S	supply voltage for the analog parts of the PCA5010 and the receiver/synthesizer control signals (Port 0 pins)
AFCOUT	18	O	Buffered analog output of DAC for automatic receiver frequency control. A voltage proportional to the offset of the receiver frequency can be generated. Can be enabled/disabled by software.
I(D1)	19	I	Input from receiver: may be demodulated NRZ signal or Zero-IF. In phase limited signal.
Q(D0)	20	I	Input from receiver: may be demodulated NRZ signal or Zero-IF. Quadrature limited signal.
V_{SSA}	21	S	ground signal reference (for the analog parts) (connected to substrate)
P0.5 to P0.7	22 to 24	I/O	**Port 0:** Port 0 is a bidirectional I/O port with internal pull-ups (option 1R, 1R, 1S, see Section 6.6.3). Port 0 pins that have logic 1s written to them are pulled HIGH by the internal pull-ups and can be used as inputs. Port 0 is also the multiplexed low-order address and data bus during access to external program and data memory. In this application, it uses strong internal pull-ups when emitting logic 1s. Port 0 also outputs the code bytes during OTP programming verification.
P1.0 to P1.2	25 to 27	I/O	**Port 1:** Port 1 is an 8-bit quasi bidirectional I/O port with internal pull-ups. Port 1 pins that have logic 1s written to them are pulled HIGH by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally pulled LOW will source current because of the internal pull-ups. (See Chapter 10: I_{pu}). P1.0 to P1.2 have external interrupts INT2 (X3) to INT4 (X5) assigned.
P1.3	28	I/O	If the UART is disabled (ENS1 in S1CON.4 = 0) then P1.3 can be used as general purpose P1 port pin. If the UART function is required, then a logic 1 must be written to P1.3. This I/O then becomes the RXD/data line of the UART.

SYMBOL	PIN	TYPE	DESCRIPTION
P1.4	29	I/O	If the UART is disabled (ENS1 in S1CON.4 = 0) then P1.4 can be used as general purpose P1 port pin. If the UART function is required, then a logic 1 must be written to P1.4. This I/O then becomes the TXD/clock line of the UART. P1.4 has external interrupt INT6 (X6) assigned.
V_{SS}	30	S	ground (connected to substrate)
V_{DD}	31	S	supply voltage for the core logic and most peripheral drivers of the PCA5010 (see V_{DDA})
ALE	32	I/O	**Address Latch Enable:** Output pulse for latching the low byte of the address during an access to external memory.
$\overline{PSEN}$	33	I/O	**Program Store Enable:** The read strobe to external program memory. When the device is executing code from the external program memory, $\overline{PSEN}$ is activated for each code byte fetch.
$\overline{EA}$	34	I/O	**External Access Enable:** $\overline{EA}$ must be externally held LOW to enable the device to fetch code from external program memory locations 0000H to 7FFFH. If $\overline{EA}$ is held HIGH, the device executes from internal program memory unless the program counter contains an address greater the 7FFFH (32 kbytes).
TCLK	35	I	clock input for use as timing reference in external access mode and emulation
V_{PP}	36	S	Programming voltage (12.5 V) for the OTP. Is connected to V_{SS} in the application.
P1.6	37	I/O	If the I^2C-bus is disabled (ENS1 in S1CON.6 = 0) then P1.6 can be used as general purpose P1 port pin. If the I^2C-bus function is required, then a logic 1 must be written to P1.6. This I/O then becomes the clock line of the I^2C-bus. P1.6 is equipped with an open-drain output buffer. The pin has no clamp diode to V_{DD}.
P1.7	38	I/O	If the I^2C-bus is disabled (ENS1 in S1CON.6 = 0) then P1.7 can be used as general purpose P1 port pin. If the I^2C-bus function is required, then a logic 1 must be written to P1.7. This I/O then becomes the data line of the I^2C-bus. P1.7 is equipped with an open-drain output buffer. The pin has no clamp diode to V_{DD}.
XTL2	39	O	output from the current source oscillator amplifier
XTL1	40	I	input to the inverting oscillator amplifier and time reference for pager decoder, real-time clock and timers
V_{BAT}	41	S	Supply terminal from battery. Is used for supplying parts of the chip that need to operate at all times.
$V_{DD(DC)}$	42	O	Supply voltage output of the DC/DC converter. An external capacitor is required.
VIND	43	I	Current input for the DC/DC converter. The booster inductor needs to be connected externally.
$V_{SS(DC)}$	44	S	ground (connected to substrate) OTP
RESETIN	45	I	Schmitt trigger reset input for the PCA5010. External R and C need to be connected to the battery supply. All internal storage elements (except microcontroller RAM) are initialized when this input is activated.

SYMBOL	PIN	TYPE	DESCRIPTION
$\overline{\text{RESOUT}}$	46	O	Monitor output for the emulation system. Is active (LOW) whenever a reset is applied to the microcontroller (a reset can be forced by RESETIN, watchdog or wake-up from DC/DC converter in off mode). A reset to the microcontroller initializes all SFRs and port pins; it has no impact on the blocks operating from V_{BAT}.
P3.2 and P3.3	47 and 48	I/O	**Port 3:** P3.2 and P3.3 are configured as push-pull output only (option 3R, see Section 6.6). Using the software input commands or the secondary port function is possible by driving the Port 3 output lines accordingly: P3.2 secondary function: $\overline{\text{INT0}}$ (external interrupt 0) P3.3 secondary function: $\overline{\text{INT1}}$ (external interrupt 1)

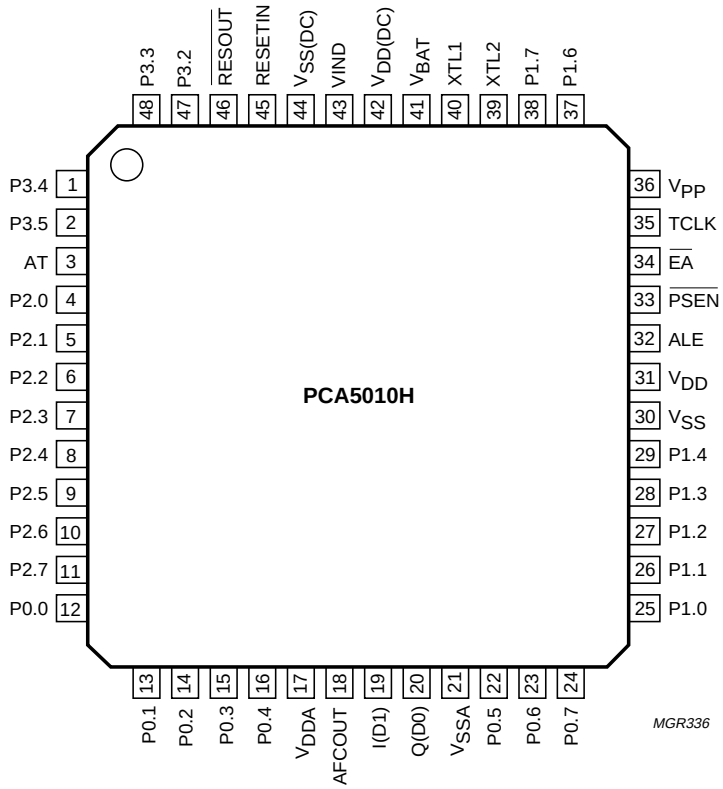


Fig.2 Pin configuration.

6 FUNCTIONAL DESCRIPTION

6.1 General

The PCA5010 contains a high-performance CMOS microcontroller and the required peripheral circuitry to implement high-speed pagers for the modern paging protocols. For this purpose, features such as FSK demodulator, protocol timer, real-time clock and DC/DC converter have been integrated on-chip.

The microcontroller embedded within the PCA5010 implements the standard 80C51 architecture and supports the complete instruction set of the 80C51 with all addressing modes.

The PCA5010 contains 32 kbytes of OTP program memory; 1.25 kbyte of static read/write data memory, 27 I/O lines, two 16-bit timer/event counters, a fifteen-source two priority-level, nested interrupt structure and on-chip oscillator and timing circuit.

The PCA5010 devices have several software selectable modes of reduced activity for power reduction; Idle for the CPU and standby or off for the DC/DC converter. The Idle mode freezes the CPU while allowing the RAM, timers, serial I/O and interrupt system to continue functioning. The standby mode for the DC/DC converter allows a high efficiency of the latter at low currents and the off mode reduces the supply voltage to the battery level. In the off mode the RAM contents are preserved, real-time clock and protocol timer are operating, but all other chip functions are inoperative.

Two serial interfaces are provided on-chip; a UART serial interface and an I^2C-bus serial interface. The I^2C-bus serial interface has byte oriented master functions allowing communication with a whole family of I^2C-bus compatible slave devices.

6.2 CPU timing

The internal CPU timing of the PCA5010 is completely different to other implementations of this core. The CPU is realized in asynchronous handshaking technology, which results in extremely low power consumption and low EMC noise generation.

6.2.1 BASICS

The implementation of the CPU of the PCA5010 as a block in handshake technology has become possible through the TANGRAM tool set, developed in the Philips Natlab in Eindhoven.

TANGRAM is a high level programming language which allows the description of parallel and sequential processes that can be compiled into logic on silicon. The CPU has the following features:

- No clock is needed. Every function within the CPU is self timed and always runs at the maximum speed that a given silicon die under the current operating conditions (supply voltage and temperature) allows.
- The CPU fetches opcodes with maximum speed until a special mode (e.g. Idle) is entered that stops this sequence.
- Only bytes that are required are fetched from the program memory. The dummy read cycles which exist in the standard 80C51 have been omitted to save power.
- To further speed up the execution of a program, the next sequential byte is always fetched from the code memory during the execution of the current command. In the event of jumps the prefetched byte is discarded.
- Since no clocks are required, the operating power consumption is essentially lower compared to conventional architectures and Idle power consumption is reduced to nearly zero (leakage only).
- Clocks are only required as timing references for timers/counters and for generating the timing to the off-chip world.

6.2.2 EXECUTION OF PROGRAMS FROM INTERNAL CODE MEMORY

When code is executed in internal access mode ($\overline{EA}$ = 1), the opcodes are fetched from the on-chip OTP. The OTP is a self timed block which delivers data at maximum speed. This is the preferred operating mode of the PCA5010.

6.2.3 EXECUTION OF PROGRAMS FROM EXTERNAL CODE MEMORY

When code is executed in external access mode ($\overline{EA}$ = 0), the opcodes are fetched from an off-chip memory using the standard signals ALE, $\overline{PSEN}$ and P0, P2 for multiplexed data and address information. In this mode the identical hardware configurations as for a standard 80C51 system can be used, even if the timing for ALE and $\overline{PSEN}$ is slightly different because it is generated from an internal oscillator.

6.3 Overview on the different clocks used within the PCA5010

Figure 3 gives an overview on the clocks available within the PCA5010 for the different functions.

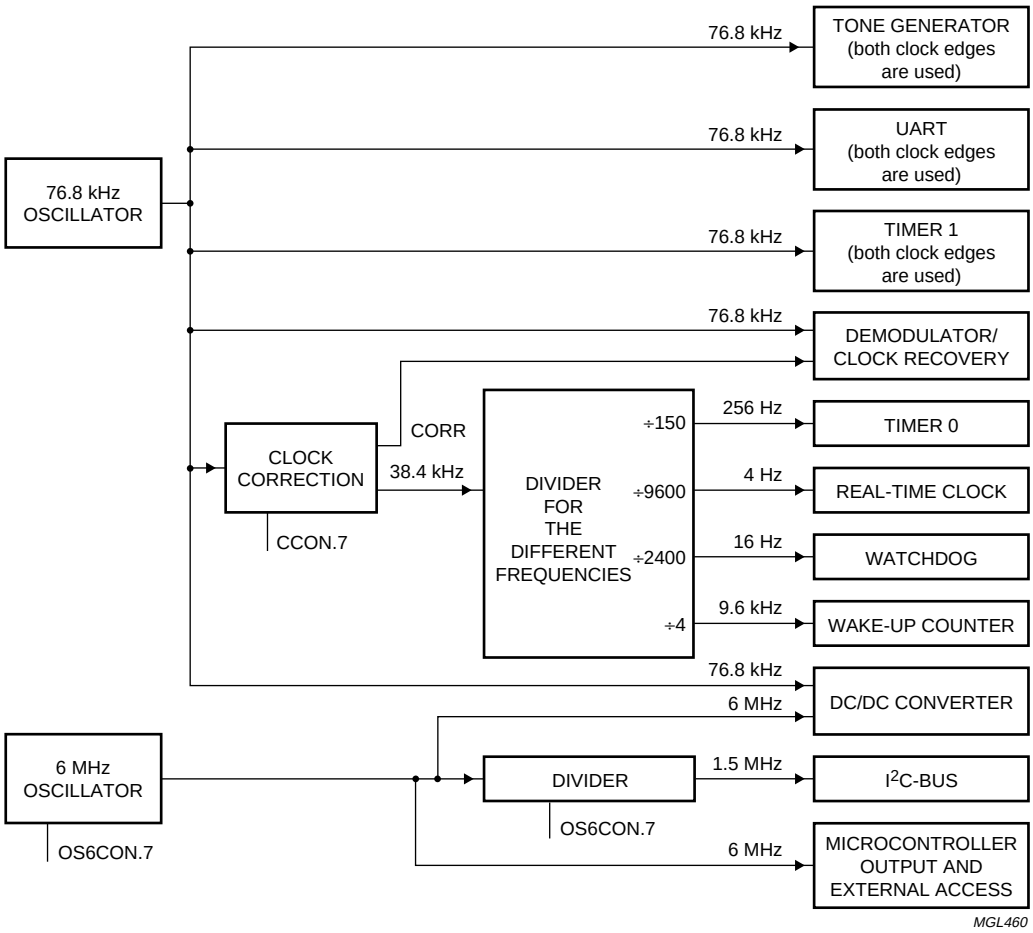


Fig.3 Overview on the clocks used within the PCA5010.

6.4 Memory organization

The PCA5010 has a program memory (OTP) plus data memory (RAM) on-chip. The device has separate address spaces for Program and Data Memory (see Fig.4). If Ports P0 and P2 are not used as I/O signals these pins can be used to address up to 64 kbytes of external program memory. In this case, the CPU generates the latch signal (ALE) for an external address latch and the read strobe ($\overline{PSEN}$) for external Program Memory. External data memory is not supported.

6.4.1 PROGRAM MEMORY

After reset the CPU begins execution of the program memory at location 0000H. The program memory can be implemented in either internal OTP or external memory. If the $\overline{EA}$ pin is strapped to V_{DD}, then program memory fetches are directed to the internal program memory. If the $\overline{EA}$ pin is strapped to V_{SS}, then program memory fetches are directed to external memory.

Programming the on-chip OTP is detailed in Chapter 15. Usually Philips will deliver programmed parts to a customer. Supply of blank engineering samples is possible, but then Philips cannot give any guarantee on the programmability and retention of the program memory.

6.4.2 DATA MEMORY

The PCA5010 contains 1280 bytes internal RAM (consisting of 256 bytes standard RAM and 1024 bytes AUX-RAM) and Special Function Registers (SFRs). Figure 4 shows the internal data memory space divided into the lower 128 bytes the upper 128 bytes and the SFR space and 1024 bytes auxiliary RAM. Internal RAM locations 0 to 127 are directly and indirectly addressable. Internal RAM locations 128 to 255 are only indirectly addressable. The SFR locations 128 to 255 bytes are only directly addressable and the auxiliary RAM is indirectly addressable as external RAM (MOVX). External Data Memory (EDM) is not supported.

6.4.3 SPECIAL FUNCTION REGISTERS

The second 128 bytes are the address locations of the special function registers. Table 1 shows the special function registers space. The SFRs include the port latches, timers, peripheral control, serial I/O registers, etc. These registers can only be accessed by direct addressing. There are 128 bit addressable locations in the SFR address space (those SFRs whose addresses are divisible by eight).

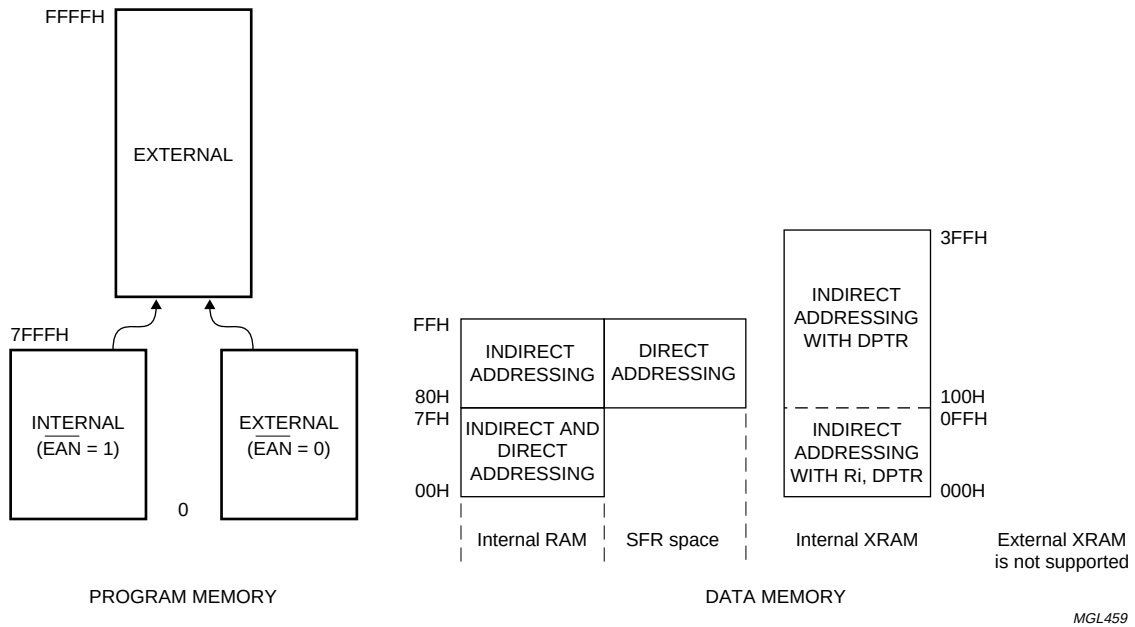


Fig.4 Memory map.

6.5 Addressing

The PCA5010 has five methods for addressing source operands:

- Register
- Direct
- Register-Indirect
- Immediate
- Base-Register plus Index-Register-Indirect.

The first three methods can be used for addressing destination operands. Most instructions have a 'destination/source' field that specifies the data type, addressing methods and operands involved.
For operations other than MOVs, the destination operand is also a source operand.

Access to memory addressing is as follows:

- Registers in one of the four 8-register banks through Register Direct or Register-Indirect
- Maximum 1280 bytes of internal data RAM through Direct or Register-Indirect
  - Bytes 0 to 127 of internal RAM may be addressed directly/indirectly. Bytes 128 to 255 of internal RAM share their address location with the SFRs and so may only be addressed Register-Indirect as data RAM.
  - Bytes 0 to 1024 of AUX-RAM can be addressed indirectly via MOVX. Bytes 256 to 1024 can only be addressed using indirect addressing with the data pointer, while bytes 0 to 255 may be also addressed using R0 or R1.
- Special function registers through Direct
- Program memory Look-Up Tables (LUTs) through Base-Register plus Index-Register-Indirect.

The PCA5010 is classified as an 8-bit device since the internal ROM, RAM, Special Function Registers (SFRs), Arithmetic Logic Unit (ALU) and external data bus are all 8-bits wide. It performs operations on bit, nibble, byte and double-byte data types.

Facilities are available for byte transfer, logic and integer arithmetic operations. Data transfer, logic and conditional branch operations can be performed directly on Boolean variables to provide excellent bit handling.

While the PCA5010 is executing code from the internal memory, ALE and $\overline{\text{PSEN}}$ pins are inactive with ALE = LOW and $\overline{\text{PSEN}}$ = HIGH.

External XRAM is not supported for this device, since P3.7 ($\overline{\text{RD}}$) and P3.6 ($\overline{\text{WR}}$) pins are not available. If the external XRAM is accessed accidentally, no $\overline{\text{PSEN}}$ or ALE cycle is done and actual P0 values are read. Internal XRAM access is not visible from outside the chip (no ALE, $\overline{\text{PSEN}}$, P0 and P2 activity).

Table 1 Special Function Registers Overview; note 1

ADDR (HEX)	NAME	7	6	5	4	3	2	1	0	R/W	RESET VALUE	COMMENT
80	P0									RW	9FH	bit addressable
81	SP									RW	07H	
82	DPL									RW	00H	
83	DPH									RW	00H	
87	PCON	SMOD	XRE	ENIS	–	GF1	GF0	PD	IDL	RW	00H	
88	TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	RW	00H	bit addressable
89	TMOD	GATE	C/T	M1	M0	GATE	C/T	M1	M0	RW	00H	
8A	TL0									RW	00H	
8B	TL1									RW	00H	
8C	TH0									RW	00H	
8D	TH1									RW	00H	
90	P1									RW	FFH	bit addressable
92	TGCON	ENB	CLK2	–	–	–	–	–	–	RW	00H	
93	TG0									RW	00H	
94	WUCON	RUN	WUP	TEST	CPL	Z1	Z0	LOAD	SET	RW	00H	see note 2
95	WUC0									RW	00H	see note 2
96	WUC1									RW	00H	see note 2
98	S0CON	SM0	SM1	–	REN	TB8	RB8	TI	RI	RW	00H	bit addressable
99	S0BUF									RW	00H	
9E	AFCON	ENB	–	AFC5	AFC4	AFC3	AFC2	AFC1	AFC0	RW	00H	
A0	P2									RW	FFH	bit addressable
A5	WDCON	COND	WD3	WD2	WD1	WD0	–	–	LD	RW	00H	
A8	IEN0/IE	EA	EWU	ES1	ES0	ET1	EX1	ET0	EX0	RW	00H	bit addressable
B0	P3									RW	C3H	bit addressable
B8	IP/IP0	–	PWU	PS1	PS0	PT1	PX1	PT0	PX0	RW	00H	bit addressable
C0	IRQ1	IQ9	IQ8	IQ7	IQ6	IQ5	IQ4	IQ3	IQ2	RW	00H	bit addressable
CD	RTCON	MIN	–	–	–	–	W/$\overline{R}$	LOAD	SET	RW	00H	see note 2
CE	RTC0									RW	00H	see note 2
D0	PSW	CY	AC	F0	RS1	RS0	OV		P[3]	RW	00H	bit addressable
D1	DCCON0	OFF	SBY	RXE	SBLI	–	–	STB[3]	BLI[3]	RW	03H	
D2	DCCON1	VBG1	VBG0	VLO1	VLO0	–	–	–	–	RW	00H	
D3	OS6CON	ENB	–	$\overline{SF4}$	SF3	SF2	SF1	SF0	MFR	RW	00H	
D4	OS6M0									R	00H	
D8	S1CON	–	ENS1	STA	STO	SI	AA	–	CR0	RW	00H	bit addressable
D9	S1STA	SC4	SC3	SC2	SC1	SC0	0	0	0	R	78H	
DA	S1DAT									RW	00H	
E0	ACC									RW	00H	bit addressable
E8	IEN1	EMIN	EWD	EDC	EX6	ESC	EX4	EX3	EX2	RW	00H	bit addressable
E9	IX1	IL9	IL8	IL7	IL6	IL5	IL4	IL3	IL2	RW	00H	

ADDR (HEX)	NAME	7	6	5	4	3	2	1	0	R/W	RESET VALUE	COMMENT
EC	DMD0	ENB	M	–	RES	LEV	BD2	BD1	BD0	RW	00H	
ED	DMD1	ENA	AVG6	AVG5	AVG4	AVG3	AVG2	AVG1	AVG0	R	00H	ENA is RW
EE	DMD2	ENC	–	BF	–	TEST	B2	B1	B0	RW	00H	
EF	DMD3									RW	00H	
F0	B									RW	00H	bit addressable
F8	IP1	PMIN	PWD	PDC	PX6	PSC	PX4	PX3	PX2	RW	00H	bit addressable
FC	CCON	ENB	PLUS	TEST	CIV17	CIV16	–	BYPAS	SET	RW	00H	
FD	CC0	CIV7	CIV6	CIV5	CIV4	CIV3	CIV2	CIV1	CIV0	RW	00H	
FE	CC1	CIV15	CIV14	CIV13	CIV12	CIV11	CIV10	CIV9	CIV8	RW	00H	

Notes

1. An empty field in this map indicates a bit that can be read or written to by software.
2. Value only reset with RESETIN and not or only partly with an off-restart sequence.
3. This bit cannot be changed by writing to it.

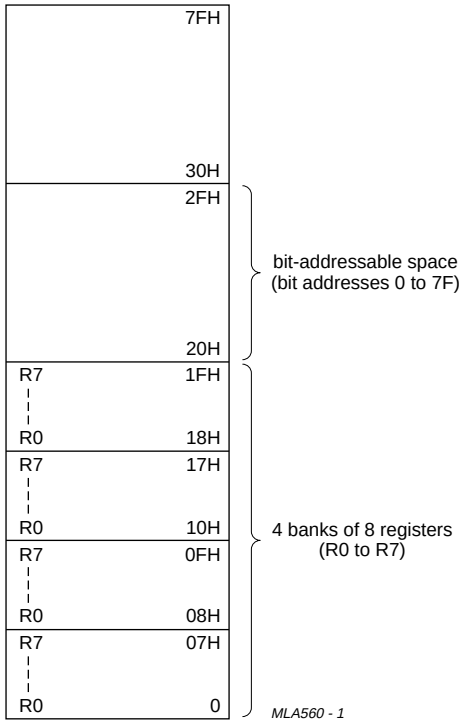


Fig.5 The lower 128 bytes of internal data memory.

6.6 I/O facilities

6.6.1 PORTS

The PCA5010 has 27 I/O lines treated as 27 individually addressable bits or as four parallel 8-bit addressable ports. Ports 0 and 2 are complete, Port 1 has only 7 and Port 3 has only 4 pins externally available. Ports 0, 1, 2 and 3 perform the following alternative functions:

Port 0 Is also used for external access, parallel OTP programming mode and emulation (see Table 2 for configuration details):

- Provides the multiplexed low-order address and data bus for expanding the device with standard memories and peripherals
- Provides access to the OTP data I/O lines in OTP parallel programming mode.

Port 1 Used for a number of alternative functions (see Table 3 for configuration details):

- Provides the inputs for the external interrupts INT2/P1.0 to INT4/P1.2 and INT6/P1.4
- SCL/P1.6 and SDA/P1.7 for the I^2C-bus interface are real open-drain outputs; no other port configurations are available
- RXD/P1.3 and TXD/P1.4 for the UART data input and output.

Port 2 Is also used for external access, parallel OTP programming mode and emulation (see Table 4 for configuration details):

- Provides the high-order address bus when expanding the device with external program memory
- Allows control of the on-chip OTP parallel programming mode.

Port 3 Pins are configured as strong push-pull outputs (see Table 5 for configuration details).
The following alternative Port 3 functions are available, but to avoid short-circuiting of the mentioned port pins, the input signals cannot be applied externally to the Port 3 pins. The alternative function can only be stimulated via the respective port output function:

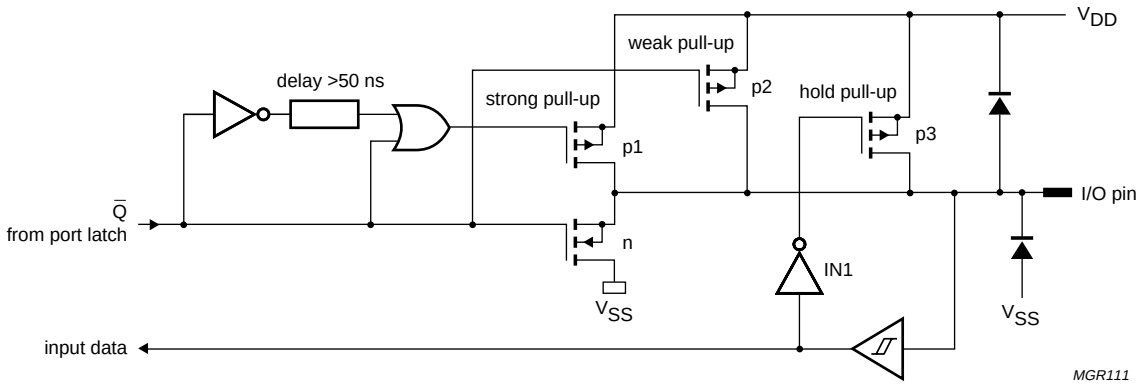
- External interrupt request inputs $\overline{INT0}$/P3.2 and $\overline{INT1}$/P3.3
- Counter inputs T0/P3.4 and T1/P3.5.

To enable a port pin alternative function, the port bit latch in its SFR must contain a logic 1.

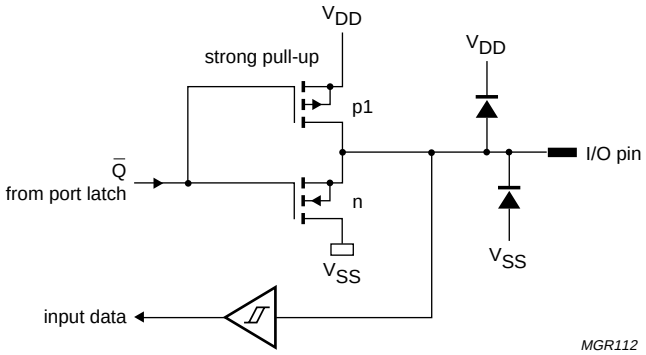
Each port consists of a latch (SFRs P0 to P3), an output driver and input buffer. Standard ports have internal pull-ups. Figure 6a shows that the strong transistor p1 is turned on for only a short time after a LOW-to-HIGH transition in the port latch. When on, it turns on p3 (a weak pull-up) through the inverter IN1. This inverter and p3 form a latch which holds the logic 1.

6.6.2 PORT I/O CONFIGURATION (OPTIONS)

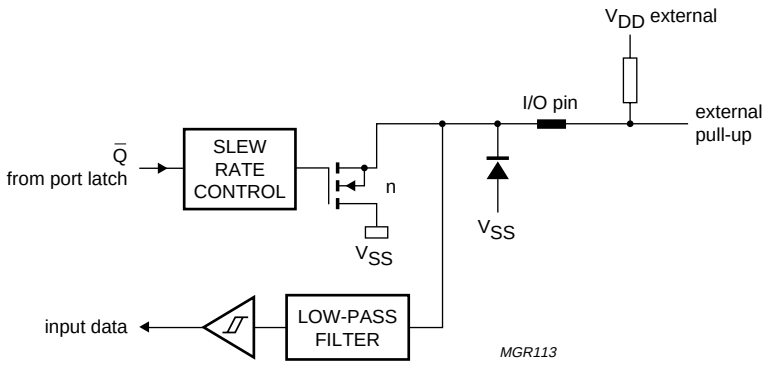
I/O port output configurations are determined on-chip according to one of the options shown in Fig.6. They cannot be changed by software.



a. Standard/quasi-bidirectional (option 1).



b. Push-pull (option 3).



c. Open-drain (only SDA/P1.7, SCL/P1.6) (option 2).

Fig.6 Port configuration options.

6.6.3 PORT I/O CONFIGURATION

Tables 2 to 6 show the hardwired configuration for the different I/Os of the PCA5010.

Table 2 Port 0 configuration; notes 1 and 2

PORT PIN	CONFIGURATION	PULL-UP	INPUT	RESET	DRIVE	POSSIBLE APPLICATION IN A PAGER
P0.0	quasi bidirectional I/O (option 1S)	yes	hys	HIGH	0.75 mA	LCD_enable (O)
P0.1	quasi bidirectional I/O (option 1S)	yes	hys	HIGH	0.75 mA	SPI_enable (O)
P0.2	quasi bidirectional I/O (option 1S)	yes	hys	HIGH	0.75 mA	SPI_clock (O)
P0.3	quasi bidirectional I/O (option 1S)	yes	hys	HIGH	0.75 mA	SPI_data (O)
P0.4	quasi bidirectional I/O (option 1S)	yes	hys	HIGH	0.75 mA	SPI_data (I)
P0.5	quasi bidirectional I/O (option 1R)	yes	hys	LOW	0.75 mA	RXE (O)
P0.6	quasi bidirectional I/O (option 1R)	yes	hys	LOW	0.75 mA	ROE (O)
P0.7	quasi bidirectional I/O (option 1S)	yes	hys	HIGH	0.75 mA	bandwidth (O)/RSSI (I)

Notes

1. Option 1S means port configuration option 1 with post-reset state set to HIGH; option 1R means post-reset state will be LOW.
2. ‘hys’ means input stage with hysteresis.

Table 3 Port 1 configuration

PORT PIN	CONFIGURATION	PULL-UP	INPUT	RESET	DRIVE	POSSIBLE APPLICATION IN A PAGER
P1.0	quasi bidirectional I/O (option 1S)	yes	hys	HIGH	0.75 mA	Key
P1.1	quasi bidirectional I/O (option 1S)	yes	hys	HIGH	0.75 mA	Key
P1.2	quasi bidirectional I/O (option 1S)	yes	hys	HIGH	0.75 mA	Key
P1.3	quasi bidirectional I/O (option 1S)	yes	hys	HIGH	0.75 mA	RXD
P1.4	quasi bidirectional I/O (option 1S)	yes	hys	HIGH	0.75 mA	TXD
P1.5	not available					
P1.6	I^2C-bus open-drain I/O (option 2S) (slew rate limited)	no	hys	HIGH	2.25 mA	SCL
P1.7	I^2C-bus open-drain I/O (option 2S) (slew rate limited)	no	hys	HIGH	2.25 mA	SDA

Table 4 Port 2 configuration

PORT PIN	CONFIGURATION	PULL-UP	INPUT	RESET	DRIVE	POSSIBLE APPLICATION IN A PAGER
P2.0	quasi bidirectional I/O (option 1S)	yes	hys	HIGH	0.75 mA	LCD_Data
P2.1	quasi bidirectional I/O (option 1S)	yes	hys	HIGH	0.75 mA	LCD_Data
P2.2	quasi bidirectional I/O (option 1S)	yes	hys	HIGH	0.75 mA	LCD_Data
P2.3	quasi bidirectional I/O (option 1S)	yes	hys	HIGH	0.75 mA	LCD_Data

PORT PIN	CONFIGURATION	PULL-UP	INPUT	RESET	DRIVE	POSSIBLE APPLICATION IN A PAGER
P2.4	quasi bidirectional I/O (option 1S)	yes	hys	HIGH	0.75 mA	LCD_Data
P2.5	quasi bidirectional I/O (option 1S)	yes	hys	HIGH	0.75 mA	LCD_Data
P2.6	quasi bidirectional I/O (option 1S)	yes	hys	HIGH	0.75 mA	LCD_Data
P2.7	quasi bidirectional I/O (option 1S)	yes	hys	HIGH	0.75 mA	LCD_Data

Table 5 Port 3 configuration

PORT PIN	CONFIGURATION	PULL-UP	INPUT	RESET	DRIVE	POSSIBLE APPLICATION IN A PAGER
P3.0	not available					
P3.1	not available					
P3.2	push-pull output (option 3R)	no	hys	LOW	3 mA	call LED
P3.3	push-pull output (option 3R)	no	hys	LOW	3 mA	vibrator
P3.4	push-pull output (option 3R)	no	hys	LOW	3 mA	back light
P3.5	push-pull output (option 3R)	no	hys	LOW	3 mA	LCD R/$\overline{W}$/RXD enable
P3.6	not available					
P3.7	not available					

The port configuration is fixed and cannot be reconfigured by software or OTP code.

Table 6 Other pins

PORT PIN	CONFIGURATION	PULL-UP	INPUT	RESET	DRIVE	POSSIBLE APPLICATION IN A PAGER
AT	push-pull output	no		LOW	3 mA	tone generator output
I(D1)	digital input	no	hys			
Q(D0)	digital input	no	hys			
TCLK	digital input	no	hys			
RESETIN	digital input	no	hys			reset input
$\overline{\text{RESOUT}}$	push-pull output	no		LOW	1.5 mA	reset output
XTL1	analog input/output (10 pF)	no	hys			to crystal quartz
XTL2	analog input/output (10 pF)	no				to crystal quartz
AFCOUT	analog output	no				
ALE	quasi bidirectional I/O	yes	hys	HIGH	1.5 mA	
$\overline{\text{PSEN}}$	quasi bidirectional I/O	yes	hys	HIGH	0.75 mA	
$\overline{\text{EA}}$	3-state I/O with bus keeper	hold	buffer	HIGH	0.75 mA	

6.7 Timer/event counters

The PCA5010 contains two 16-bit timer/event counters: Timer 0 and Timer 1 which can perform the following functions:

- Measure time intervals and pulse durations
- Count events
- Generate interrupt requests
- Generate output on comparator match
- Generate a Pulse Width Modulated (PWM) output signal.

Timer 0 and Timer 1 can be programmed independently to operate in four modes:

Mode 0 8-bit timer or 8-bit counter each with divide-by-32 prescaler.

Mode 1 16-bit time interval or event counter.

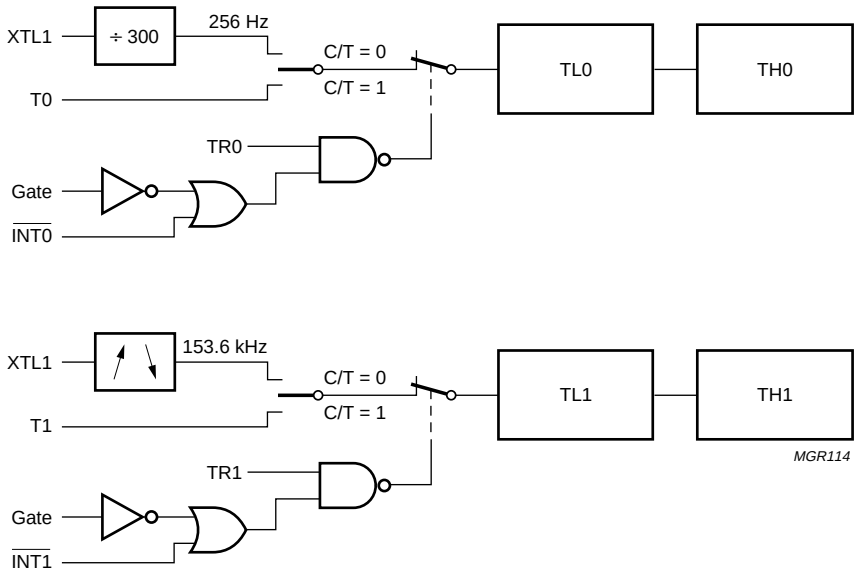
Mode 2 8-bit time interval or event counter with automatic reload upon overflow.

Mode 3 this mode of the standard 80C51 is not available.

In the timer mode the timers count events on the XTL1 input. Timer 0 counts through a prescaler at a rate of 256 Hz and Timer 1 counts directly on both edges of the XTL1 signal at a rate of 153.6 kHz. The nominal frequency of the XTL1 signal is 76.8 kHz.

In the counter mode the register is incremented in response to a HIGH-to-LOW transition at P3.4 (T0) and P3.5 (T1).

Besides the different input frequencies and the non-availability of Mode 3, both Timer 0 and Timer 1 behave exactly identical to the standard 80C51 Timer 0 and Timer 1.



Detailed configuration of the 4 available modes is found in the 80C51 family hardware description (*"Philips Semiconductors IC20 Data Handbook"*).

Fig.7 Timer/counter 0 and 1: clock sources and control logic.

6.8 I²C-bus serial I/O

The serial port supports the 2-line I²C-bus which consists of a data line (SDA) and a clock line (SCL). These lines also function as the I/O port lines P1.7 and P1.6 respectively. The system is unique because data transport, clock generation, address recognition and bus control arbitration are all controlled by hardware. The I²C-bus serial I/O has complete autonomy in byte handling. The implementation in the PCA5010 operates in single master mode as:

- Master transmitter
- Master receiver.

These functions are controlled by the S1CON register. S1STA is the status register whose contents may also be used as a vector to various service routines. S1DAT is the data shift register. The block diagram of the I²C-bus serial I/O is shown in Fig.8.

6.8.1 Differences to a standard I²C-bus interface

The I²C-bus interface of the PCA5010 implements the standard for master receiver and transmitter as defined in e.g. P83CL781/782 with the following restrictions:

- The baud rate is fixed to either 100 kHz (CR0 = 0) or 400 kHz (CR0 = 1) derived from the on-chip 6 MHz oscillator. Therefore bits CR1 and CR2 in the S1CON SFR are not available.
- Only single master functions are implemented.
  - Slave address (S1ADR) is not available
  - Status register (S1STA) reports only status defined for the MST/TRX and MST/REC modes
  - Multimaster operation is not supported.

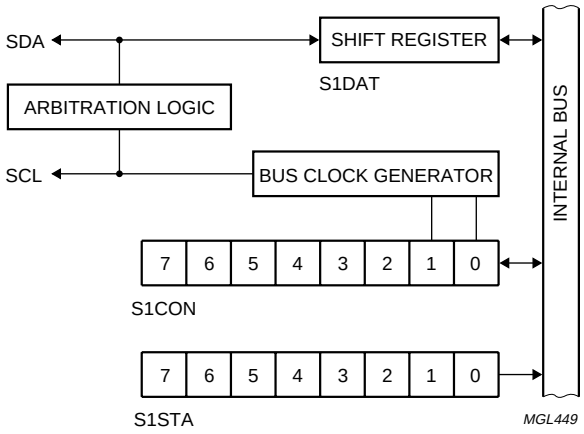


Fig.8 Block diagram of I²C-bus serial I/O.

6.8.2 TIMING

The timing of the I²C-bus interface is based on the internal 6 MHz clock. The phases of this clock divided-by-4 are used as a reference in the 400 kHz mode and divided-by-16 in the 100 kHz mode. In the following context 'T' (333 ns or 1.33 μs) denotes a single phase of this clock.

The transfer of a single bit lasts 9 T. SCL is HIGH for 5 T. When receiving data, the PCA5010 samples the SDA line after 3 T while SCL is HIGH.

The implemented I²C-bus Interface operates according to the timing diagram in Fig.9.

The open-drain I²C-bus outputs are implemented as slew rate controlled driver stages, to minimize the negative impact of I²C-bus activity on the pager sensitivity while the pager is receiving. Typical waveforms on P1.7 (SDA) and P1.6 (SCL) are shown in Fig.10.

Because SDA and SCL are open-drain type I/Os, only the falling edge is determined by the driver characteristics. The static sink current when driving LOW and the slope of the rising edges are determined by the capacitive I²C-bus load and its resistive termination (pull-up to V_{DD}).

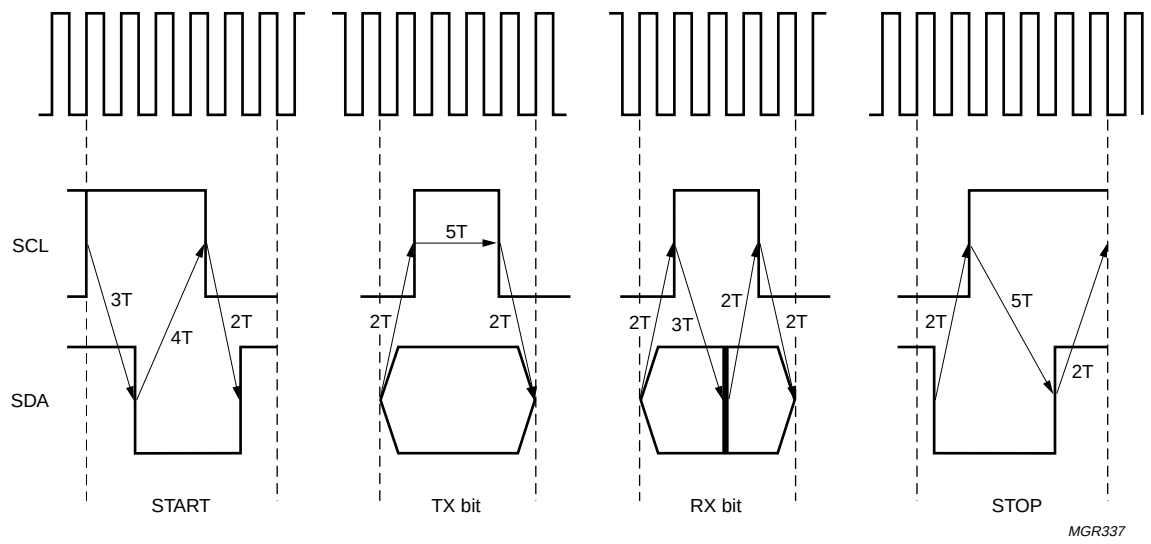
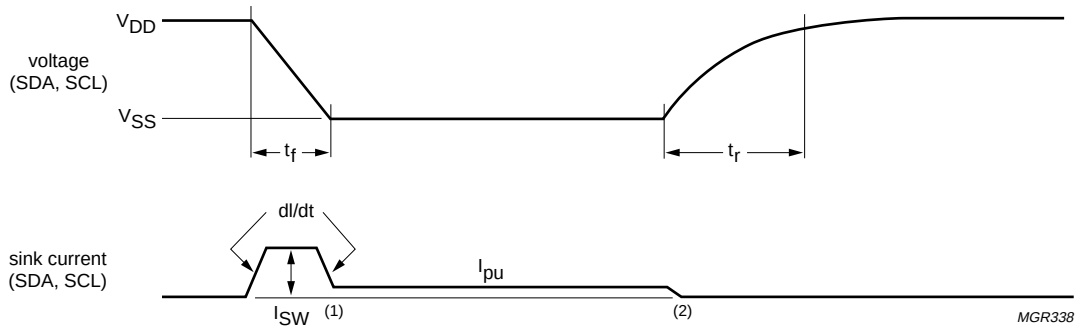


Fig.9 Timing of the I²C-bus interface.



(1) The falling slope depends on the capacitive load. Typical values at 2.2 V where C_L = 50 pF are: t_f = 100 ns; I_{SW} = 2 mA; dI/dt = 250 µA/ns.
(2) The rising slope is defined by external pull-up resistor and capacitive load (a typical t_r is 1 µs at 50 pF/20 kΩ.

Fig.10 Typical waveforms on SDA and SCL.

6.8.3 SERIAL CONTROL REGISTER (S1CON)

Table 7 Serial Control Register (S1CON, SFR address D8H)

7	6	5	4	3	2	1	0
–	ENS1	STA	STO	SI	AA	–	CR0

Table 8 Description of the S1CON bits

BIT	SYMBOL	FUNCTION
S1CON.7	–	CR2 is not available.
S1CON.6	ENS1	**Enable serial I/O**. When ENS1 = 0, the serial I/O is disabled. SDA and SCL outputs are in the high-impedance state; P1.6 and P1.7 function as open-drain ports. When ENS1 = 1, the serial I/O is enabled. Output port latches P1.6 and P1.7 must be set to logic 1.
S1CON.5	STA	**START flag**. If STA is set while the SIO is in master mode, SIO will generate a repeated START condition.
S1CON.4	STO	**STOP flag**. With this bit set while in master mode a STOP condition is generated. When a STOP condition is detected on the I^2C-bus, the SIO hardware clears the STO flag.
S1CON.3	SI	**SIO interrupt flag**. This flag is set, and an interrupt is generated, after any of the following events occur: • A START condition is generated in master mode • A data byte has been received or transmitted in master mode (even if arbitration is lost). If this flag is set, the I^2C-bus is halted (by pulling down SCL). Received data is only valid until this flag is reset.
S1CON.2	AA	**Assert Acknowledge**. When this bit is set, an acknowledge (LOW level to SDA) is returned during the acknowledge clock pulse on the SCL line when: • A data byte is received while the device is programmed to be a master receiver. When this bit is reset, no acknowledge is returned.
S1CON.1	–	CR1 is not available.
S1CON.0	CR0	Speed selection (with on-chip 6 MHz oscillator tuned to 6 MHz the nominal bus frequency is: CR0 = 0 is 83.3 kHz (6 MHz divided-by-72) CR0 = 1 is 333 kHz (6 MHz divided-by-18).

6.8.4 Data Shift Register (S1DAT)

S1DAT contains the serial data to be transmitted or data which has just been received. Bit 7 is transmitted or received first; i.e. data shifted from left to right.

Table 9 Data Shift Register (S1DAT, SFR address DAH)

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

6.8.5 Address Register (S1ADR)

The slave address register is not available since slave mode is not supported.

6.8.6 SERIAL STATUS REGISTER (S1STA)

The contents of this register may be used as a vector to a service routine. This optimizes the response time of the software and consequently that of the I^2C-bus. S1STA is a read-only register. The status codes for all available modes of a single master I^2C-bus interface are given in Tables 12 to 14.

Table 10 Serial Status Register (S1STA and SFR address D9H)

7	6	5	4	3	2	1	0
SC4	SC3	SC2	SC1	SC0	0	0	0

Table 11 Description of the S1STA bits

BIT	SYMBOL	FUNCTION
S1STA.3 to S1STA.7	SC4 to SC0	5-bit status code
S1STA.0 to S1STA.2	–	these 3 bits are held LOW

Table 12 MST/TRX mode

S1STA VALUE	DESCRIPTION
08H	a START condition has been transmitted
10H	a repeated START condition has been transmitted
18H	SLA and W have been transmitted, ACK has been received
20H	SLA and W have been transmitted, $\overline{\text{ACK}}$ received
28H	DATA of S1DAT has been transmitted, ACK received
30H	DATA of S1DAT has been transmitted, $\overline{\text{ACK}}$ received

Table 13 MST/REC mode

S1STA VALUE	DESCRIPTION
40H	SLA and R have been transmitted, ACK received
48H	SLA and R have been transmitted, $\overline{\text{ACK}}$ received
50H	DATA has been received, ACK returned
58H	DATA has been received, $\overline{\text{ACK}}$ returned

Table 14 Miscellaneous

S1STA VALUE	DESCRIPTION
78H	no information available (reset value); the serial interrupt flag SI, is not yet set

Table 15 Symbols used in Tables 12 to 14

SYMBOL	DESCRIPTION
SLA	7-bit slave address
R	read bit
W	write bit
ACK	acknowledgement (acknowledge bit = logic 0)
$\overline{ACK}$	no acknowledgement (acknowledge bit = logic 1)
DATA	8-bit data byte to or from I^2C-bus
MST	master
SLV	slave
TRX	transmitter
REC	receiver

6.9 Serial interface SIO0: UART

The UART interface of the PCA5010 implements a subset of the complete standard as defined in e.g. the P80CL580.

6.9.1 Differences to the standard 80C51 UART

The following deviations from the standard exist:

- If [SM1 and SM0] = 10 then Mode 1 (8-bit data transmission) is selected, with a fixed baud rate (4800/9600 bits/s)
- If [SM1 and SM0] = 01 then Mode 2 (9-bit data transmission) is selected, with a fixed baud rate (4800/9600 bits/s)
- Modes 0 and 3 and the variable baud rate selection using Timer 1 overflow is not available
- The SM2 bit has no function
- The time reference for modes 1 and 2 is taken from the 76.8 kHz oscillator, instead of the original $\frac{f_{OSC}}{12}$

6.9.2 UART modes

This serial port is full duplex which means that it can transmit and receive simultaneously. It is also receive-buffered and can commence reception of a second byte before a previously received byte has been read from the register. However, if the first byte has not been read by the time the reception of the second byte is complete, the second byte will be lost. The serial port receive and transmit registers are both accessed via the special function register S0BUF. Writing to S0BUF loads the transmit register and reading S0BUF accesses a physically separate receive register.

The serial port can operate in 2 modes:

Mode 1 10 bits are transmitted (through TXD) or received (through RXD): a START bit (0), 8 data bits (LSB first) and a stop bit (1). On receive, the stop bit goes into RB8 in special function register S0CON (see Figs 11 and 12).

Mode 2 11 bits are transmitted (through TXD) or received (through RXD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit and a STOP bit (1). On transmit, the 9th data bit (TB8 in S0CON) can be assigned the value of 0 or 1. Or, for example, the parity bit (P, in the PSW) could be moved into TB8. On receive, the 9th data bit goes into RB8 in S0CON, while the STOP bit is ignored (see Figs 11 and 13).

In both modes the baud rate can be selected to either 4800 or 9600 depending on the SMOD bit in the PCON SFR. If SMOD = 0 the baud rate is 4800, if SMOD = 1 the baud rate is 9600 with a 76.8 kHz quartz.

In both modes, transmission is initiated by any instruction that uses S0BUF as a destination register. Reception is initiated by the incoming start bit if REN = 1.

6.9.3 Serial Port Control Register (S0CON)

The serial port control and status register is the special function register S0CON (see Table 16). The register contains not only the mode selection bits, but also the 9th data bit for transmit and receive (TB8 and RB8), and the serial port interrupt bits (TI and RI).

Table 16 Serial Port Control Register (S0CON, SFR address 98H)

7	6	5	4	3	2	1	0
SM0	SM1	–	REN	TB8	RB8	TI	RI

Table 17 Description of the S0CON bits

BIT	SYMBOL	FUNCTION
S0CON.7	SM0	this bit along with the SM1 bit, is used to select the serial port mode; see Table 18
S0CON.6	SM1	this bit along with the SM0 bit, is used to select the serial port mode; see Table 18
S0CON.5	–	SM2 is not available
S0CON.4	REN	this bit enables serial reception and is set by software to enable reception, and cleared by software to disable reception
S0CON.3	TB8	this bit is the 9th data bit that will be transmitted in Mode 2; set or cleared by software as desired
S0CON.2	RB8	in Mode 2, this bit is the 9th data bit received; in Mode 1 it is the stop bit that was received
S0CON.1	TI	**The transmit interrupt flag**. Set by hardware at the end of the 8th bit time in Mode 0, or at the beginning of the stop bit time in the other modes, in any serial transmission. Must be cleared by software.
S0CON.0	RI	**The receive interrupt flag**. Set by hardware at the end of the 8th bit time in Mode 0, or halfway through the stop bit time in the other modes, in any serial transmission (for exception see SM2). Must be cleared by software.

Table 18 Selection of the serial port modes

SM0	SM1	MODE	DESCRIPTION	BAUD RATE
0	1	1	8-bit UART	$\frac{1}{16}f_{osc}$ or $\frac{1}{8}f_{osc}$
1	0	2	9-bit UART	$\frac{1}{16}f_{osc}$ or $\frac{1}{8}f_{osc}$

6.9.4 UART DATA REGISTER (S0BUF)

S0BUF contains the serial data to be transmitted or data which has just been received. Bit 0 is transmitted or received first.

Table 19 Data Shift Register (S0BUF, SFR address 99H)

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

6.9.5 BAUD RATES

The baud rate in Modes 1 and 2 depends on the value of the SMOD bit in SFR PCON and may be calculated as:

$$\text{Baud rate} = \frac{2^{SMOD}}{16} \times f_{osc}$$

- If SMOD = 0, (which is the value on reset), the baud rate is $\frac{1}{16}f_{osc}$
- If SMOD = 1, the baud rate is $\frac{1}{8}f_{osc}$.

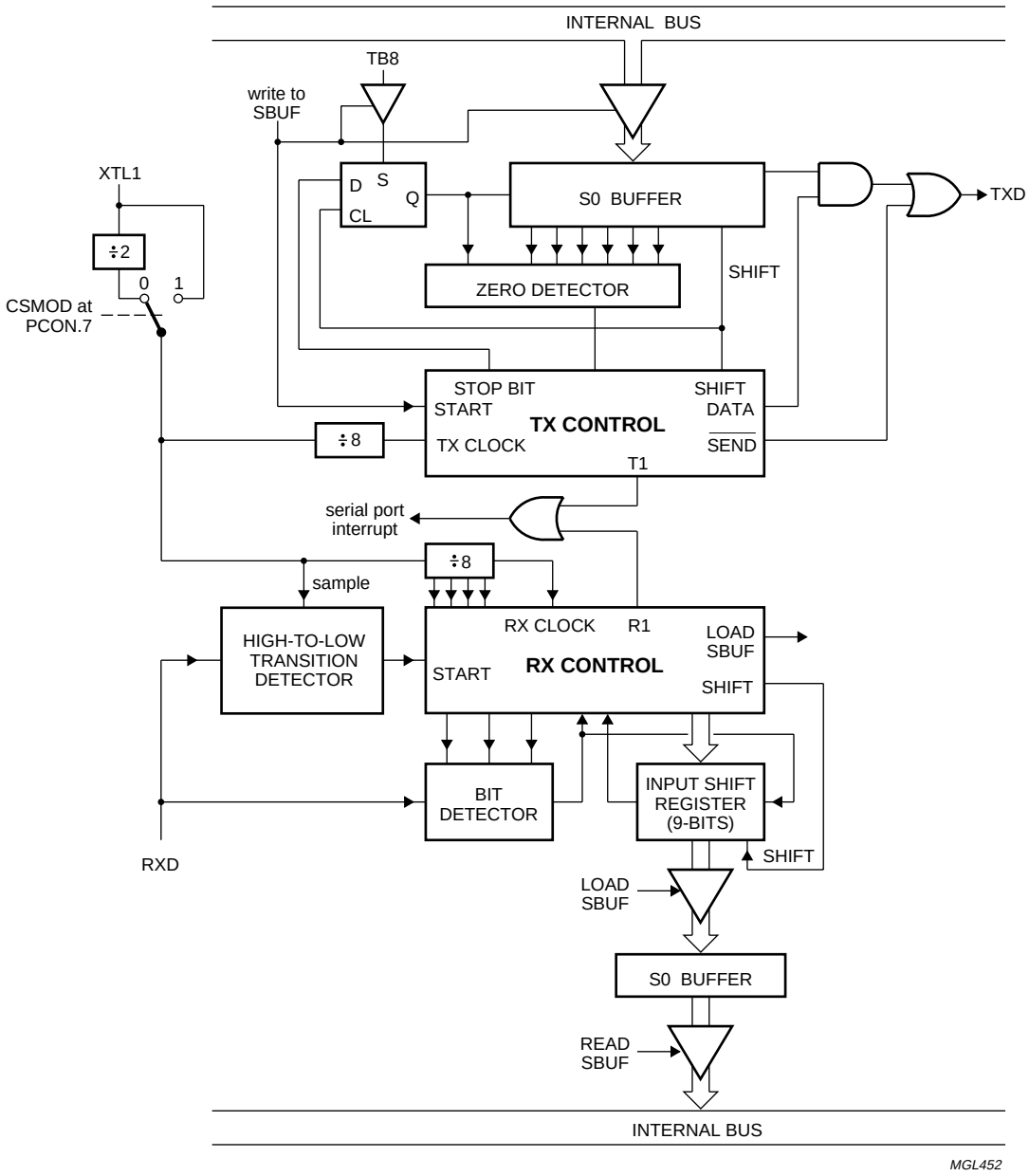


Fig.11 Serial port Mode 1 and Mode 2.

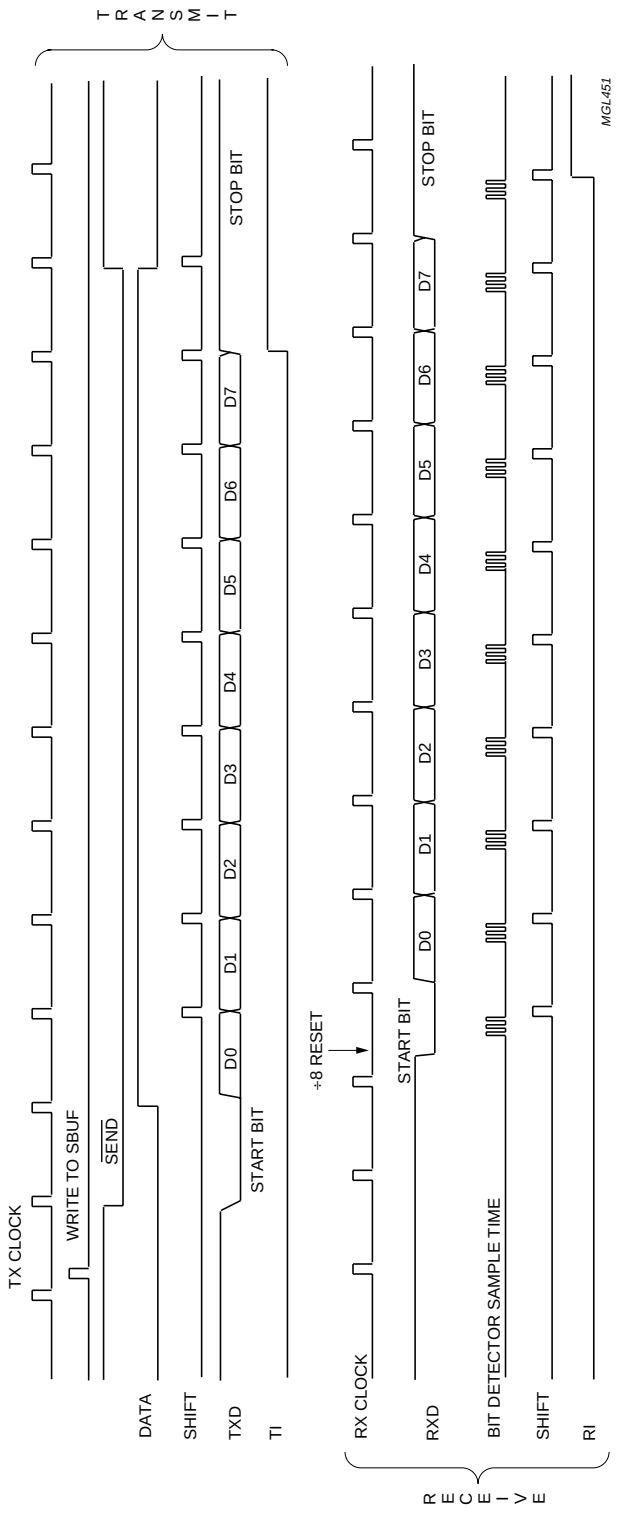


Fig.12 Serial port Mode 1 timing.

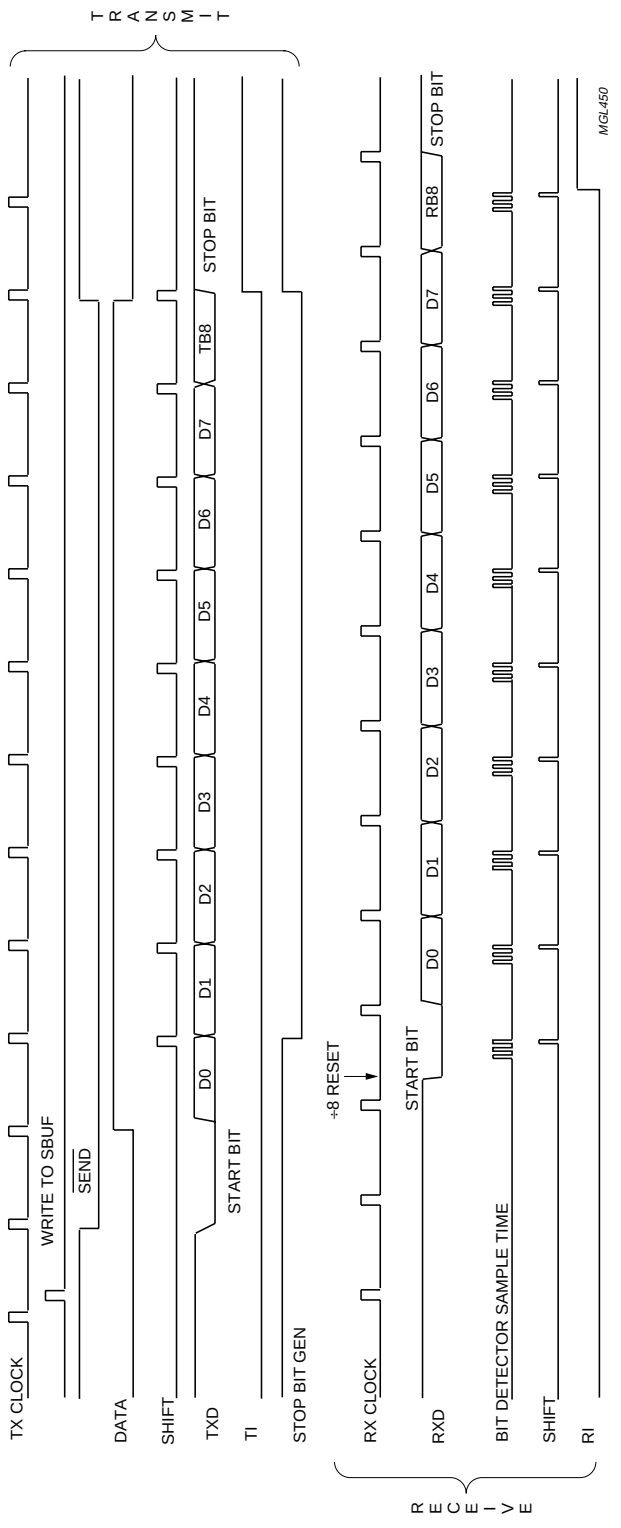


Fig.13 Serial port Mode 2 timing.

6.10 76.8 kHz oscillator

6.10.1 FUNCTION

The oscillator produces a reference frequency of 76.8 kHz. The frequency offset is compensated by a separate digital clock correction block. The oscillator operates directly on V_{BAT} and is always enabled.

6.10.2 OSCILLATOR CIRCUITRY

The on-chip inverting oscillator amplifier is a single NMOS transistor supplied with a constant current. The amplitude visible at terminals XTL1 and XTL2 is therefore not a full rail swing with a very high impedance. To reduce the power consumption, the input Schmitt trigger buffer is limited to approximately 100 kHz maximum frequency. The whole circuit operates directly at the battery supply. The 76.8 kHz oscillator cannot be disabled. It also continues its operation during DC/DC converter off or 80C51 stop mode.

The simplest application configuration is shown in Fig.14a. C1 and C2 can be added to operate a crystal at its optimal load condition. The resulting capacitance of the series connection of C1 and C2 must be smaller than 5 pF for a guaranteed start-up of the oscillator.

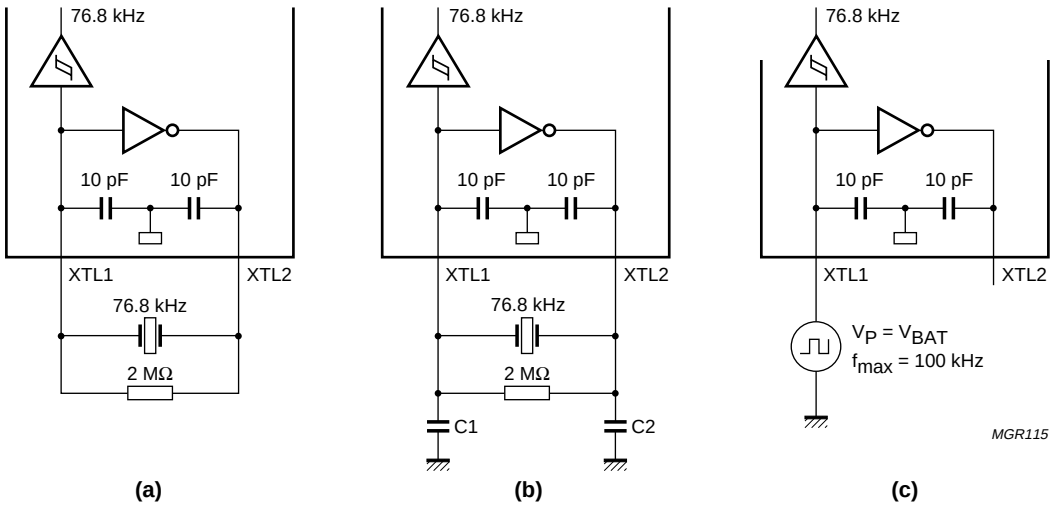


Fig.14 Oscillator circuit.

6.11 Clock correction

6.11.1 FUNCTION

The clock correction block is connected to the 76.8 kHz oscillator. It operates directly on V_{BAT}. By means of the clock correction circuit a digital adjustment of the 76.8 kHz oscillator signal is implemented.

An 18-bit interval counter inserts or deletes one pulse from the 76.8 kHz clock each time its count has expired.
The interval is stored by the processor to the 18-bit interval register CIV. Addition/deletion is performed by hardware.

Crystal offset correction can be performed with a resolution of 5 ppm.

This block also generates the timing reference signals for other functional blocks such as the RTC (4 Hz), watchdog (16 Hz), Timer 0 (256 Hz), wake-up counter (9600 Hz) and the demodulator/clock recovery block. The generation of these timing references is always active and cannot be disabled.

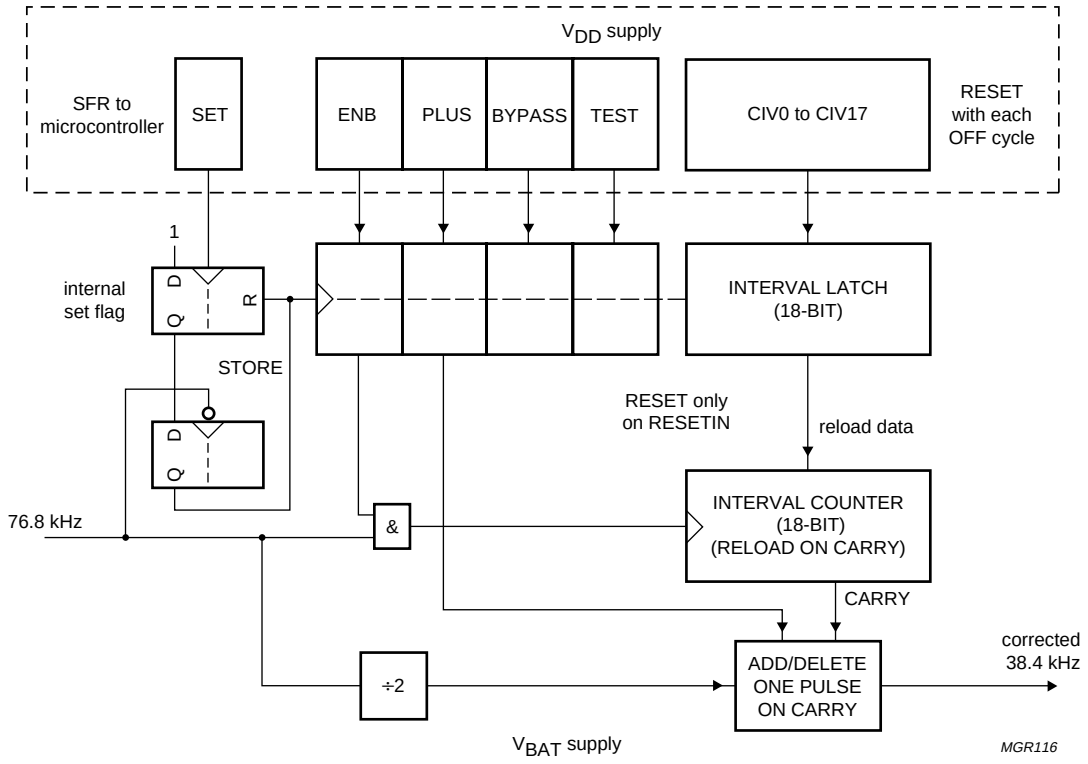


Fig.15 Block diagram of clock compensation.

6.11.2 Clock Correction Control Register (CCON)

The CCON special function register is used to control the clock correction by software.

Table 20 Clock Correction Control Register (CCON, SFR address FCH)

7	6	5	4	3	2	1	0
ENB	PLUS	TEST	CIV17	CIV16	–	BYPASS	SET

Table 21 Description of the CCON bits

BIT	SYMBOL	FUNCTION
CCON.7	ENB	**Enable clock correction**. If ENB = 1 has been set, then correction is enabled and will stay enabled even when the DC/DC converter is shut down and restarted.
CCON.6	PLUS	± **Sign for value**. If PLUS = 1 then clock pulses are inserted, or else deleted.
CCON.5	TEST	**Test signal**, must always be logic 0 in normal mode. It is used during test to bypass the first 9 FFs in the timing generator divider chain. If TEST = 1 the clock rate of the signals 9600 Hz and 256 Hz is doubled and the frequency on 16 Hz and 4 Hz is multiplied by 300.
CCON.4	CIV17	bit 17 of interval value, is used as extension of CC0 and CC1
CCON.3	CIV16	bit 16 of interval value, is used as extension of CC0 and CC1
CCON.2	–	unused.
CCON.1	BYPASS	**Test signal**, must always be logic 0 in normal mode. It is used during test to generate 76.8 kHz on all outputs of the timing generator (4 Hz, 16 Hz, 256 Hz and 9600 Hz).
CCON.0	SET	**A load signal to the interval register**. After a logic 0 to logic 1 transition of this bit the value of ENB, PLUS, TEST, BYPASS and CIV are copied into the local latches with the next 76.8 kHz clock pulse. A duration of one MOV instruction is long enough for the set operation to complete. The SFR values must remain stable for at least one oscillator period because the actual transfer happens synchronized with the local clock (see Figs 16 and 18).

6.11.3 Clock Correction Interval Registers (CC0 and CC1)

The CC0 and CC1 special function registers (together with CCON.3 and CCON.4) are used to define the interval between subsequent clock correction actions.

Table 22 Clock Correction Interval Register (CC0, SFR address FDH)

7	6	5	4	3	2	1	0
CIV7	CIV6	CIV5	CIV4	CIV3	CIV2	CIV1	CIV0

Table 23 Clock Correction Interval Register (CC1, SFR address FEH)

7	6	5	4	3	2	1	0
CIV15	CIV14	CIV13	CIV12	CIV11	CIV10	CIV9	CIV8

6.11.4 EXAMPLE SEQUENCE TO SET ANOTHER CLOCK CORRECTION INTERVAL

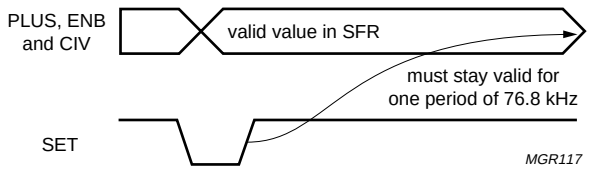


Fig.16 Sequence for setting the clock compensation.

MOV CC0, #(CIV7 to CIV0)

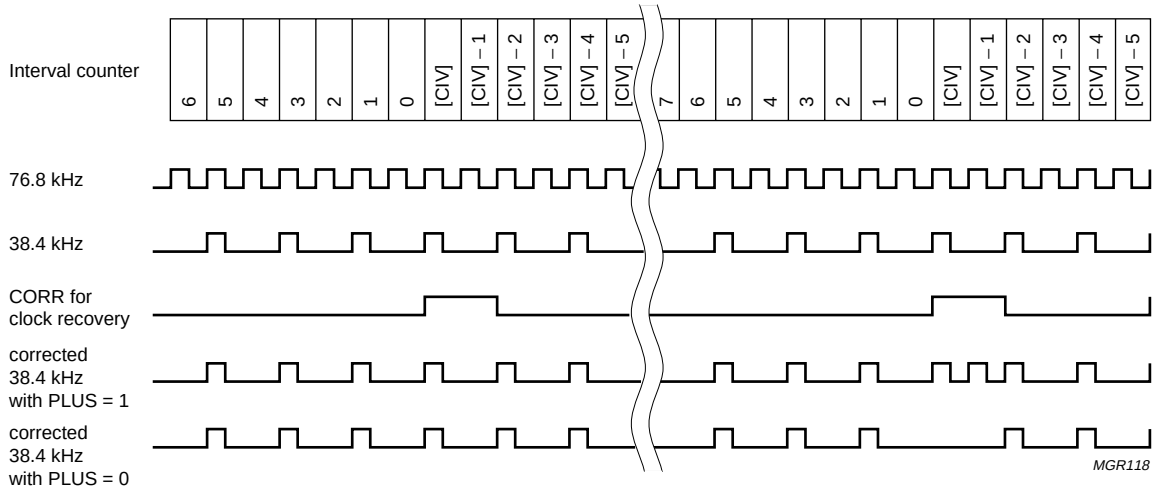
MOV CC1, #(CIV8 to CIV15)

MOV CCON, #D4H

MOV CCON, #D5H.

6.11.5 TIMING

Figures 17 and 18 demonstrate how the clock correction works and how the access of the microcontroller is synchronized to the local operation.



After (CIV) clock ticks of 76.8 kHz or 38.4 kHz one correction is made.

Fig.17 Operation of clock compensation.

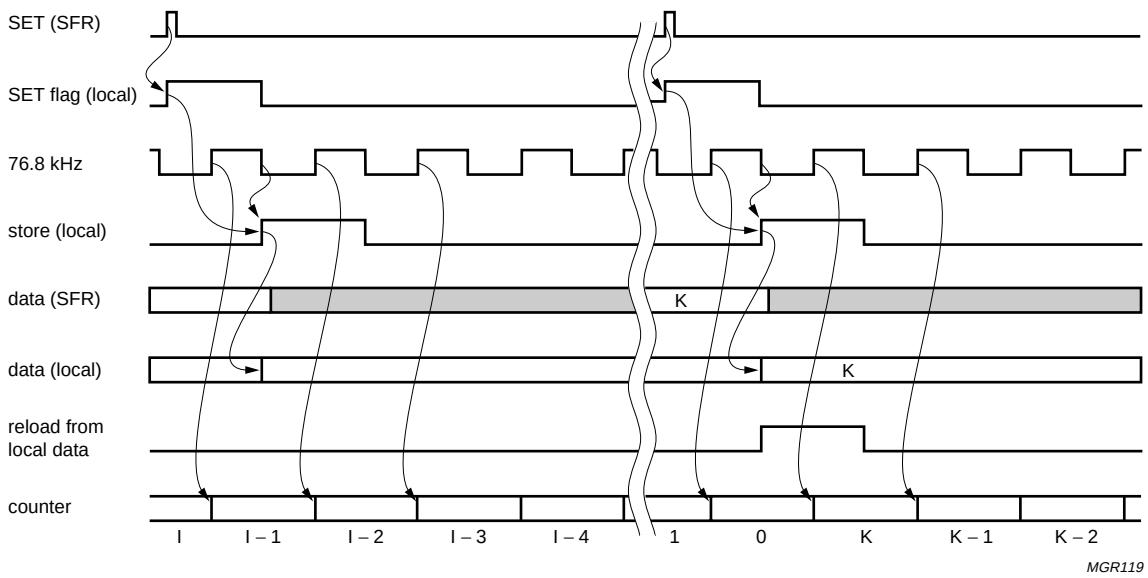


Fig.18 Synchronization of local counter operation and access from the microcontroller.

6.12 6 MHz oscillator

6.12.1 FUNCTION

The 6 MHz oscillator provides the clock for the DC/DC converter, the I²C-bus interface, the port I/Os and for the external memory access timing (ALE/$\overline{\text{PSEN}}$).

The 6 MHz oscillator is a 5 inverter stage current controlled ring oscillator. The oscillator is optimized for low operating current consumption.

The actual frequency of the oscillator can be measured by activating the MFR signal. An 8-bit counter will then be reset and will start counting at the first rising edge of the 76.8 kHz signal and stop counting at the next rising edge of the 76.8 kHz signal. The processor then can read the contents of the MFR counter.

The processor can adjust the oscillator frequency using the F0 to F4 signals (control of source current for ring oscillator).

The 6 MHz oscillator is enabled by hardware only during the start-up phase and whenever the DC/DC converter needs the 6 MHz clock. In all other cases the 6 MHz oscillator is switched of by hardware.

The DC/DC converter does not need the 6 MHz clock when set in standby mode.

If the 6 MHz output is required as a frequency source for other blocks (e.g. I²C-bus) the software needs to enable it explicitly by setting ENB = 1. Besides the DC/DC converter the following functions require the operation of the 6 MHz oscillator:

- I²C-bus block as basic time reference
- Port output logic. Software commands that write to the ports need this clock to complete the operation (if a program ‘hangs’, this could be the problem).
- Code fetching from external memories needs the clock for the ALE/$\overline{\text{PSEN}}$ timing (e.g. LJMP 5000H needs this clock for completion).

When the ENB bit has been set by software, the clock will be available internally after the start-up time of this oscillator. The start-up time is 2 to 3 periods of the 76.8 kHz reference frequency.

6.12.2 6 MHz Oscillator Control Register (OS6CON)

The OS6CON special function register is used to control the operation of the on-chip 6 MHz oscillator. The 6 MHz oscillator can be controlled as follows:

- It can be enabled or disabled. Disabling this oscillator when the DC/DC converter is in standby mode and no port I/O nor I^2C-bus activity is required saves current.
- The frequency of the oscillator can be adjusted by setting the SFx bits accordingly
- The actual frequency of this oscillator can be measured by writing the MFR bit to logic 1.

Table 24 6 MHz Oscillator Control Register (OS6CON, SFR address D3H)

7	6	5	4	3	2	1	0
ENB	–	$\overline{SF4}$	SF3	SF2	SF1	SF0	MFR

Table 25 Description of the OS6CON bits

BIT	SYMBOL	FUNCTION
OS6CON.7	ENB	**Enable oscillator**. If ENB = 1 then the function is enabled. The enable bit is only cleared when the processor writes the bit to logic 0, or if the DC/DC converter is put into 'OFF' state and a reset is generated during the following power-up sequence.
OS6CON.6	–	unused
OS6CON.5	$\overline{SF4}$	**Set frequency**. This 5-bit value adjusts the current of the ring oscillator and thus the frequency. Writing a small value decreases the frequency. The nominal frequency of 6 MHz is assigned to code ($\overline{SF4}$, SF3, SF2, SF1, SF0) = 00000. The resolution of the frequency adjustment is 200 kHz per step, the range is approximately 3 to 9 MHz. In order to start with the nominal frequency the MSB is inverted in this SFR.
OS6CON.4	SF3	
OS6CON.3	SF2	
OS6CON.2	SF1	
OS6CON.1	SF0	
OS6CON.0	MFR	**Measure frequency**. If a positive pulse is issued on this SFR-bit a frequency measurement cycle is executed. The duration of this cycle is one period of 76.8 kHz. The count of 6 MHz periods during the measurement cycle is reported back in OS6M0. The bit must be reset by software.

6.12.3 6 MHz Oscillator Measured Frequency Register (OS6M0)

The actual frequency of the 6 MHz on-chip oscillator can be calculated from the value in the OS6M0 special function register, after a Measure Frequency operation (MFR).

Table 26 6 MHz Oscillator Measured Frequency Register (OS6M0, SFR address D4H)

7	6	5	4	3	2	1	0
MF7	MF6	MF5	MF4	MF3	MF2	MF1	MF0

The value stored in this SFR is the counted number of 6 MHz cycles during one 76.8 kHz period. The frequency of the 6 MHz oscillator is therefore f = MF $\times$ 76800 Hz with a resolution of 76800 Hz.

6.12.4 ENABLING OF THE 6 MHZ OSCILLATOR

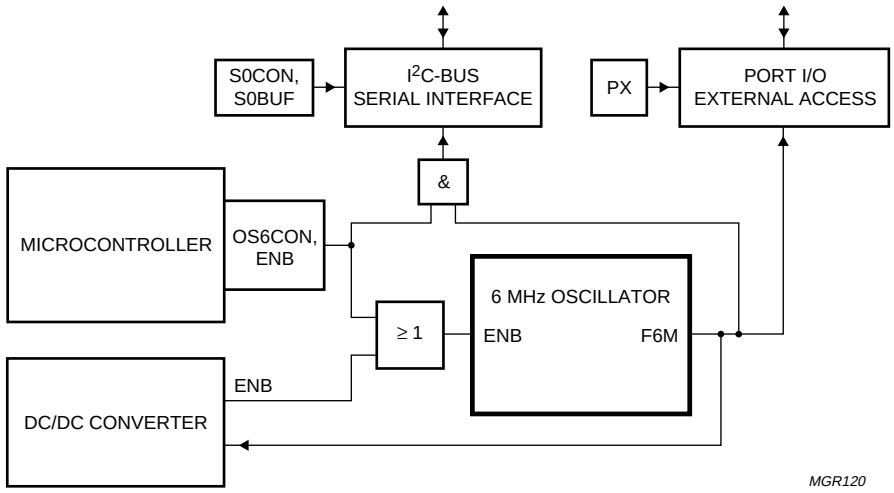


Fig.19 Relationship between 6 MHz oscillator, DC/DC converter and microcontroller.

6.13 Real-time clock

6.13.1 FUNCTION

The real-time clock consists of an 8-bit counter that is active at all times. To save power it is operated directly on V_{BAT}. It counts up on every 4 Hz clock pulse (corrected clock).

The RTC can be read from and written to by the processor. When it reaches 239, the signal MINUTE is activated. This signal resets the counter to 0 (at the next clock pulse), and generates an MIN-interrupt for the processor.

The microcontroller 'sees' the minute interrupt as if it was an X9 interrupt. It can be enabled and disabled and must be cleared as an X9 interrupt (CLR IQ9).

If the DC/DC converter is not active when this happens, the DC/DC converter is started first and a power-up/restart sequence of the microcontroller follows. The MIN bit remains set during this procedure.

6.13.2 REAL-TIME CLOCK CONTROL REGISTER (RTCON)

The RTCCON special function register is used to control the operation of the on-chip real-time clock function.

Table 27 RTC Control Register (RTCCON, SFR address CDH)

7	6	5	4	3	2	1	0
MIN	–	–	–	–	W/$\overline{R}$	LOAD	SET

Table 28 Description of the RTCON bits

BIT	SYMBOL	FUNCTION
RTCON.7	MIN	**MIN is activated when the counter reaches 239**. MIN is used to generate the interrupt request signal MINUTE. In order to complete the interrupt cycle and reset the interrupt source, the processor has to clear MIN. This must be done in a 2 step operation writing MIN and then applying a positive edge to SET.
RTCON.6	–	unused
RTCON.5	–	unused
RTCON.4	–	unused
RTCON.3	–	unused
RTCON.2	W/$\overline{R}$	Before the RTC time can be set by software, the updating of the SFR by the RTC must be disabled. This is done by writing the W/$\overline{R}$ bit to logic 1. The W/$\overline{R}$ bit is cleared by hardware after the next 4 Hz clock, when the RTC has been loaded with its next value.
RTCON.1	LOAD	**Load RTC with contents of RTC0**. LOAD is sampled with the positive edge of the set flag SET. If LOAD is not HIGH during a SET operation, only the MIN flag is (re)set by the command.
RTCON.0	SET	**Latch signal for the real-time clock**. With the pulse on SET the content of MIN is copied into the ‘real’ MIN latch. This is necessary because the RTC has to be active at all times independant of the microcontroller.

6.13.3 Real-Time Clock Data Register (RTC0)

Table 29 RTC Data Register (RTC0, SFR address CEH)

7	6	5	4	3	2	1	0
QSECS7	QSECS6	QSECS5	QSECS4	QSECS3	QSECS2	QSECS1	QSECS0

The value stored in this SFR is the actual 4 Hz count since the last MINUTE interrupt. The contents of this counter can be read from and written to by software. The contents of this counter are only initialized when RESETIN is activated. During an OFF sequence, the RTC continues its operation.

The value of the RTC data register is only updated while the STB flag in the DCCON0 SFR is HIGH, i.e. the DC/DC converter is able to sustain the V_{DD} supply voltage. If the STB flag is logic 0 the real-time clock continues its operation, the MINUTE interrupt occurs regularly, but the SFR is not updated.

6.13.4 Example sequence for programming the RTC:

Sequence to set another value into the RTC:

MOV RTCON, #06H; set LOAD, W/$\overline{R}$ bits

MOV RTC0, #(new value); load new RTC value into SFR

MOV RTCON, #07H; now set the data valid flag (SET) in the SFR.

Sequence to clear an interrupt of the RTC:

CLR IQ9; Interrupt request flag is IQ9

MOV RTCON, #00H; clear also MIN flag in the SFR

MOV RTCON, #01H; now set the data valid flag (SET) in the SFR.

6.13.5 Timing

The interface between 2 and 1 V regions is implemented similar to the clock correction block. The sequence for writing values is identical (see Fig.15).

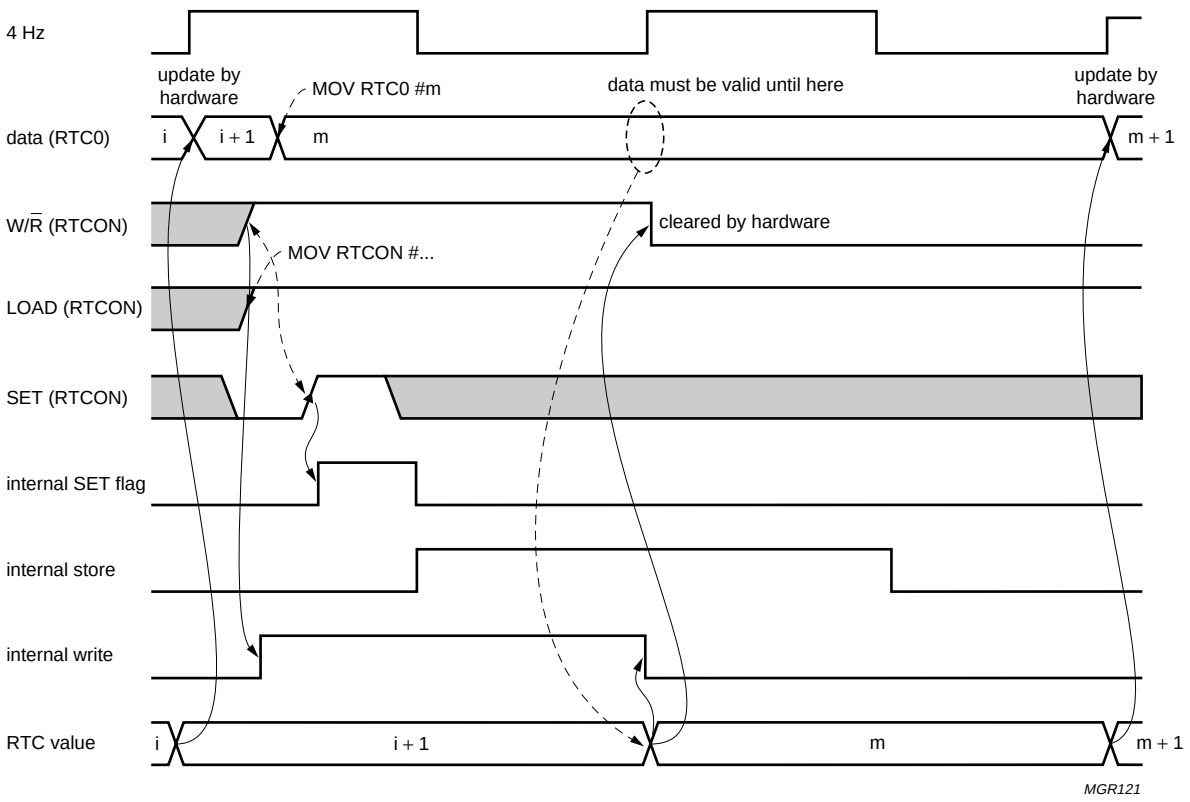


Fig.20 Operation of RTC to microcontroller interface.

6.14 Wake-up counter

6.14.1 FUNCTION

The wake-up counter is intended to be used as protocol timer. It can be programmed to wake-up the processor when the protocol needs an action. Amongst others this may be:

- Switching on the DC/DC converter at time 0
- Enabling the receiver at time 1
- Enabling the demodulator and clock recovery function at time 2 before relevant data is expected.

The time to wake-up is defined as a 16-bit value containing the number of 9600 Hz ticks. The maximum time interval that can be spawn with one cycle then equals 6.8 s.

The wake-up counter and it's reload latch are supplied by V_{BAT} and work independent of the 2 V supply. A reset to the microcontroller does not clear the wake-up counter control flags or the reload latch, but clears the reload register (see Fig.21).

The counter is implemented as a 16-bit ripple down counter. It can be loaded from the wake-up reload latch by a signal from the processor. When the counter is loaded it automatically starts if the RUN signal is active. When the counter reaches zero the wake-up signal becomes active and may generate an interrupt. The wake-up signal automatically reloads the counter (modulo N counter). The counter is stopped when the RUN signal is written to logic 0. Auto reloading of the counter is also possible, when the DC/DC converter is not operating (i.e. V_{DD} is below 1.8 V).

The contents of the wake-up counter cannot be read by the processor. Reading WUC0 and WUC1 reflects the contents of the 16-bit wake-up register (set by the microcontroller).

The interface between 2 and 1 V regions is implemented similar to the clock correction block. The sequence for writing values is identical (see Fig.16).

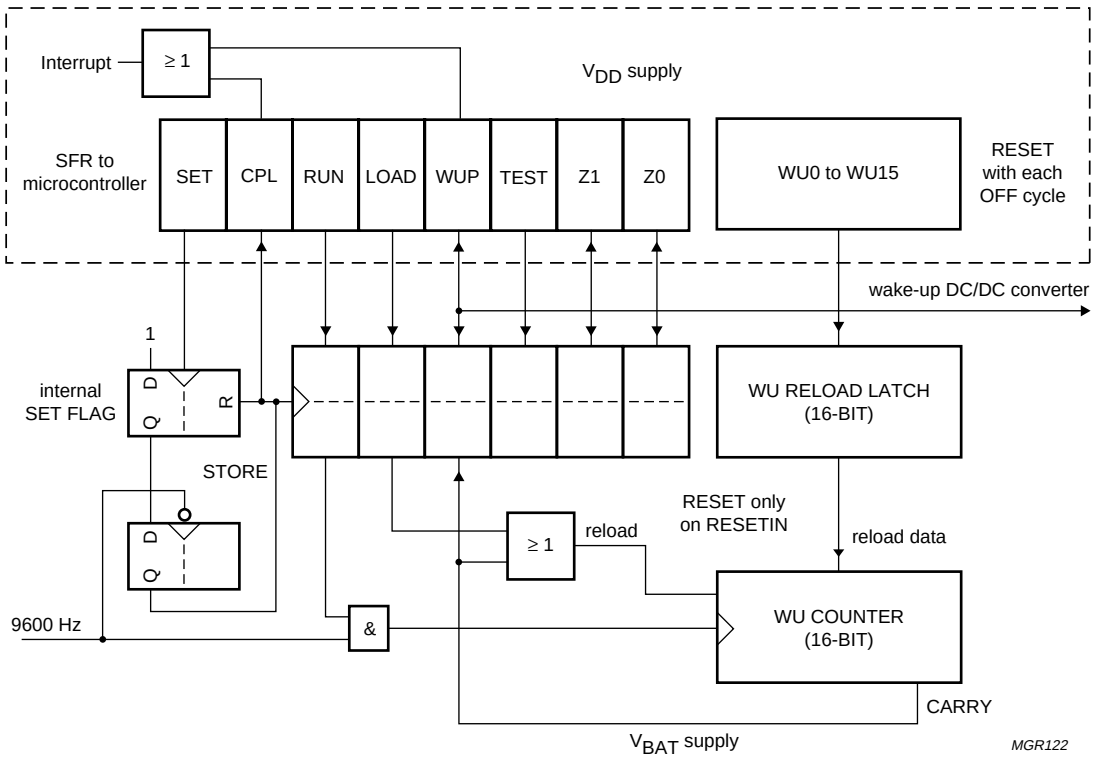


Fig.21 Block diagram of wake-up counter.

6.14.2 Wake-Up Counter Control Register (WUCON)

The WUCON special function register is used to control the operation of the wake-up counter by software.

Table 30 Wake-up Counter Control Register (WUCON, SFR address 94H)

7	6	5	4	3	2	1	0
RUN	WUP	TEST	CPL	Z1	Z0	LOAD	SET

Table 31 Description of the WUCON bits

BIT	SYMBOL	FUNCTION
WUCON.7	RUN	Control signal from the processor.
WUCON.6	WUP	**Latched wake-up signal**. The bit is set by hardware (or software) and generates a wake-up interrupt if enabled and the DC/DC converter STB-bit is set. The bit needs to be cleared by software (SFR and 1 V bits). A SET sequence is required to clear the flag on the 1 V side. Attention: reading the bit reads the contents of the 'real' wake-up flag on the 1 V side (read/modify/write commands will fail on this bit).
WUCON.5	TEST	**Test control signal**. (uses 76.8 kHz as clock input for high and low counter).
WUCON.4	CPL	**Set operation completed**. Bit set by hardware when the last operation is completed and the SFRs are again ready to accept new settings. The bit generates a wake-up interrupt if enabled. The bit needs to be cleared by software.
WUCON.3	Z1	2 bits that are only reset by a primary RESETIN. The bits can be written to and read from by the software. The bits are not cleared when the DC/DC converter is switched off. Same procedure for setting the bits as WU0 to WU15 (reading these bits returns the 'real' flags on the 1 V side; read/modify/write commands will fail on this bit).
WUCON.2	Z0	
WUCON.1	LOAD	**Load wake-up counter with contents of reload latch** (see Fig.21). Is sampled on the positive edge of SET.
WUCON.0	SET	Clock signal for writing to RUN or wake-up SFR (on 1 V level).

6.14.3 Wake-Up Data Registers (WUC0 and WUC1)

The WUC0 and WUC1 special function registers are used to define the interval to the next wake-up interrupt.

Table 32 Low Wake-Up Register (WUC0, SFR address 95H)

7	6	5	4	3	2	1	0
WU7	WU6	WU5	WU4	WU3	WU2	WU1	WU0

Table 33 High Wake-Up Register (WUC1, SFR address 96H)

7	6	5	4	3	2	1	0
WU15	WU14	WU13	WU12	WU11	WU10	WU9	WU8

WU0 to WU15 is a 16-bit register that is loaded by the processor. The contents of this register will be loaded into a 16-bit reload latch with a positive pulse on SET and into the 16-bit ripple down counter with a positive pulse on LOAD.

The value stored in the wake-up counter cannot be read by software. The contents of this counter are only initialized when RESETIN is activated. During an off sequence the wake-up counter continues its operation.

The wake-up-interrupt can only occur while the STB flag in the DCCON0 SFR is HIGH, i.e. the DC/DC converter is able to sustain the V_{DD} supply voltage. If the STB flag is logic 0 the wake-up counter continues its operation, the wake-up flag is set when expired (and can still be checked by software), but an interrupt is not generated.

6.14.4 Example sequence for controlling the wake-up counter

Sequence to set another reload value:

MOV WUC1, #(high VALUE)

MOV WUC0, #(low VALUE)

MOV WUCON, #82H; set RUN and LOAD bit

MOV WUCON, #83H; activate SET flag

MOV PCON, #01H; >>> IDLE, WAIT FOR CPL INTERRUPT.

6.14.5 Timing

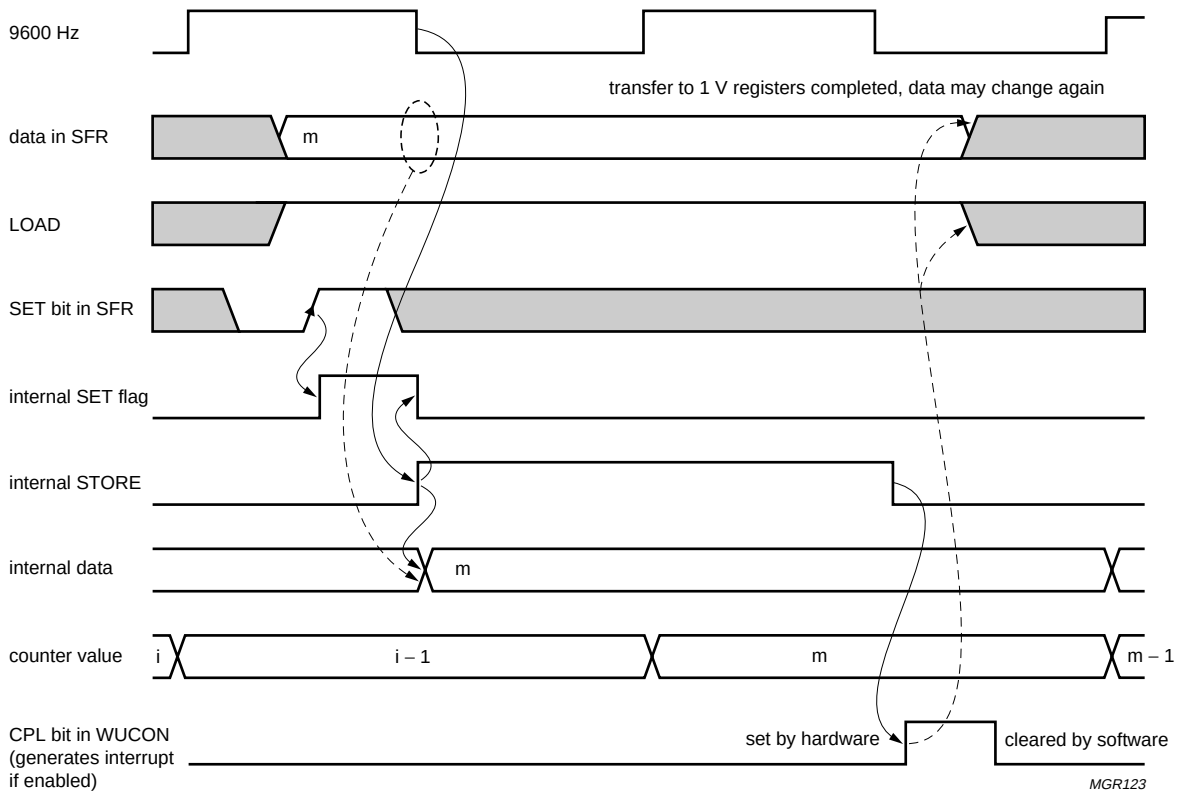


Fig.22 Operation of wake-up counter to microcontroller interface.

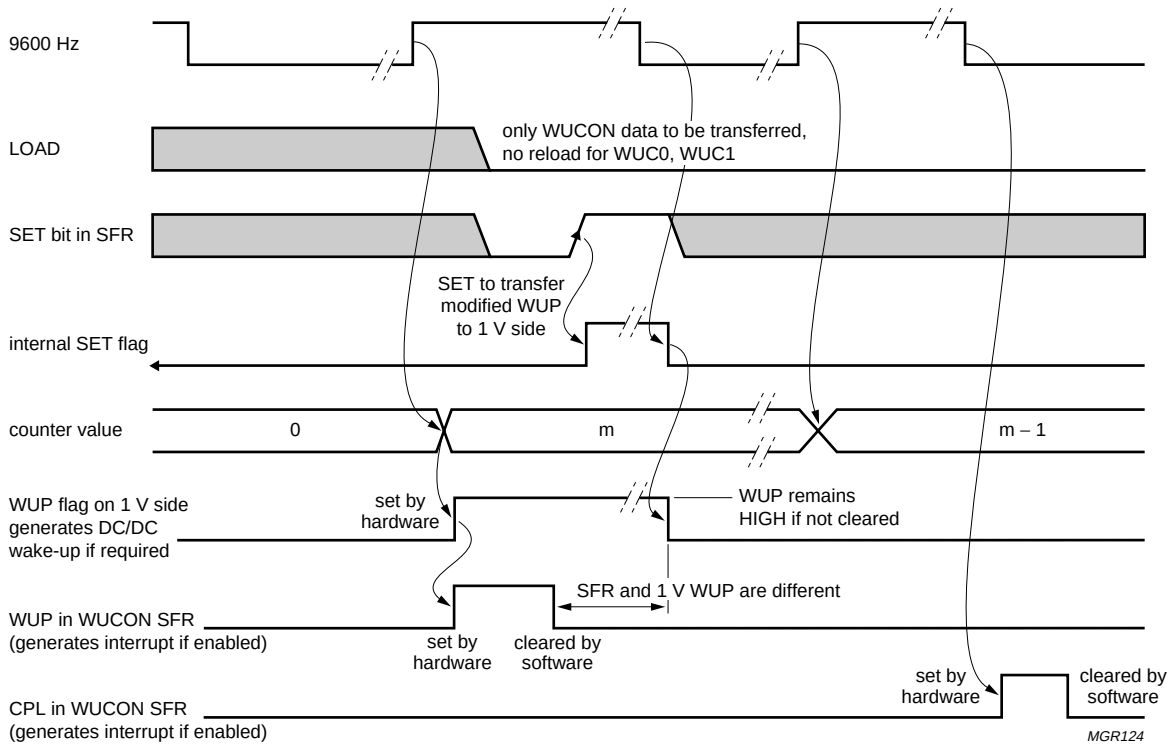


Fig.23 Wake-up interrupt sequence.

6.15 Tone generator

6.15.1 FUNCTION

The tone generator is implemented by a programmable divider from 76.8 kHz. An 8-bit value is used to define the cycle of a modulo N counter. The output of the modulo N counter is divided-by-2 to produce a symmetrical output signal. The counter is running when enabled.

The output frequency at the pin AT is defined as: $f_{AT} = \frac{76.8\ kHz}{TFREQ}$ if TFREQ ≥ 1. If TFREQ = 0 then f_{AT} = 76.8 kHz.

A secondary clock signal can be used as clock input to the modulo N counter. This input is required to generate the accurate resonance frequency of certain acoustic alerters (e.g. 512, 687, 1024, 1365, 2048, 2730 or 4096).

The tone volume can be controlled by setting the frequency on or off alerter resonance.

6.15.2 INTERFACES

SFR ADDR.	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TGCON (92H)	ENB	CLK2	–	–	–	–	–	–
TG0 (93H)	TFREQ7	TFREQ6	TFREQ5	TFREQ4	TFREQ3	TFREQ2	TFREQ1	TFREQ0

SFR:

- TFREQ0 to TFREQ7: 8-bit register containing the divisor of the tone. Loaded by the processor.
- ENB: enable frequency generator. Control signal from processor.
- CLK2: use secondary clock input for tone generation. If set a 32768 Hz clock signal is generated from the primary 76800 Hz clock signal and used as a timing reference for the tone generator.

Inputs:

- 76.8 kHz: Input to the tone counter.

Outputs:

- AT Output for alerter. Is logic 0 when disabled:

$$f_{AT} = \frac{76.8\ kHz}{TFREQ}$$

6.15.3 Generation of the 32768 Hz reference

The 32768 Hz reference is generated from 76800 Hz according to the following algorithm:

```
forever do
   begin
     for 10 times do {
       from 7 clocks on 76.8 kHz generate
       3 pulses on 32 kHz
     }
     from 5 clocks on 76.8 kHz generate
     2 pulses on 32 kHz
   end
```

6.16 Watchdog timer

6.16.1 Function

The watchdog timer consists of an 8-bit down counter. The binary number defined with WD3 to WD0 defines the expiration time of the watchdog timer between 1 to 16 s. Once enabled this counter is running continuously. Once expired the timer produces firstly an interrupt and finally a reset. The software must reload the watchdog in regular intervals to avoid expiration.

A positive edge on the LD SFR bit (re)loads the counter with the value of WD3 to WD0, sets the LOW bits to logic 1 and activates this counter if it is not yet running. However, to prepare the (re)loading a positive edge must be applied to the COND bit in WDCON. In this way at least two locations in software must be passed before the counter can be reloaded.
After reset the counter is not running. Only after the first LD it is clocked continuously by a clock pulse of 16 Hz until the DC/DC converter is switched off or an external reset is applied.

If the next LD signal is not given within the defined expiry interval an overflow occurs and the processor will be reset (signal WDR). 1 clock cycle before the reset is applied an WDI interrupt is issued. This gives the opportunity to avoid the reset if required. The maximum watchdog expiry time is thus 254×16 Hz ticks to the WD interrupt and 255×16 Hz ticks to the reset. If the DC/DC converter is in the off mode, the watchdog timer is suspended.

6.16.2 Watch Dog Timer Control Register (WDCON)

The WDCON special function register is used to control the operation of the on-chip watchdog timer.

Table 34 Watchdog Control Register (WDCON, SFR address A5H)

7	6	5	4	3	2	1	0
COND	WD3	WD2	WD1	WD0	–	–	LD

Table 35 Description of the WDCON bits

BIT	SYMBOL	FUNCTION
WDCON.7	COND	**Load condition**. Control signal from processor.
WDCON.6	WD3	WD0 to WD3 is the preset value for the high nibble of the watchdog timer. The value is the number of seconds to expiry of the watchdog.
WDCON.5	WD2	
WDCON.4	WD1	
WDCON.3	WD0	

BIT	SYMBOL	FUNCTION
WDCON.2	–	unused
WDCON.1	–	unused
WDCON.0	LD	**Load watchdog timer with WD0 to WD3**. Control signal from processor.

6.16.3 SAMPLE SEQUENCE TO RELOAD THE WATCHDOG

The sequence to reload the watchdog with 1 s is:

MOV WDCON, #80H; prepare condition

MOV WDCON, #01H; reload the timer.

6.17 2 or 4-FSK demodulator, filter and clock recovery circuit

6.17.1 FUNCTION

The aim of the blocks demodulator and clock recovery circuitry is to take the signal from the receiver, to format it into symbols and to transfer it to the processor. The two blocks use the 76.8 kHz clock.

The demodulator decodes the incoming signal and generates a sequence of NRZ data. This data is fed to the clock recovery block which regenerates the synchronization clock. This clock is used to sample and to shift the symbols into the register DMD3. Each block is enabled separately. To save power, the functions should be disabled whenever not needed.

6.17.1.1 Demodulator and filter

The demodulator can operate both with 2-level or 4-level FSK input signals (selectable by means of bit LEV).
For both types of input signals the so called demodulator, filter and direct modes are allowed. The operation mode is selected on the basis of M bit and BF bit.

In the demodulator mode (M = 0 and BF = X) the I and Q signals are decoded according to Table 36.

Operating in this mode, an offset compensation can be performed and the calculated offset value is stored into register DMD1, in the field AVG. The offset value can be used by the processor to adjust the analog AFC output voltage.

The offset coding is given in Table 37.

The performance of the demodulator for the different baud rates in 2L mode is shown in Fig.24 and for 4L mode in Fig.25. The graphs show the Bit Error Rate (BER) as a function of Eb/No (ratio of signal energy per bit to average noise power per unit bandwidth).

Both the filter and direct modes are intended for application with an external demodulator. In this case NRZ data is fed to the I and Q pins. In the 4-FSK case, the MSB is at pin I and the LSB is at pin Q. In the 2-FSK situation, only the I pin is used while pin Q must be connected to V_{SS}. In these two modes, the offset calculation and compensation cannot be performed.

In the filter mode (M = 1 and BF = 0), the data is filtered and then sent to the clock recovery. The filter characteristics of the implemented filter are shown in Fig.26.

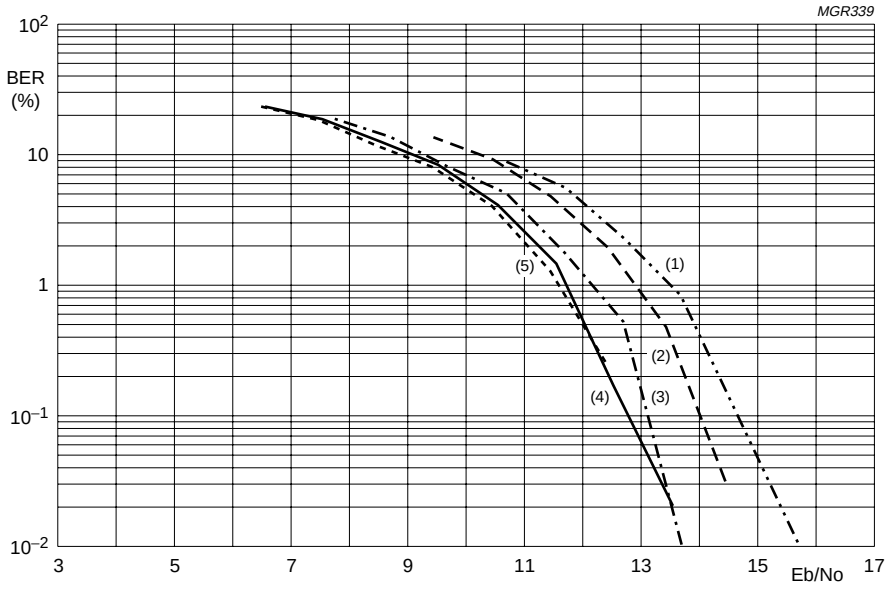
In the direct mode (M = 1 and BF = 1), no function of the demodulator is performed. Consequently there is no filtering on the data which is sent directly to the clock recovery.

Table 36 Modulation coding

FREQUENCY (Hz)	2-FSK		4-FSK	
	D1	D0	D1	D0
+4800	1	X	1	0
+1600	1	X	1	1
−1600	0	X	0	1
−4800	0	X	0	0

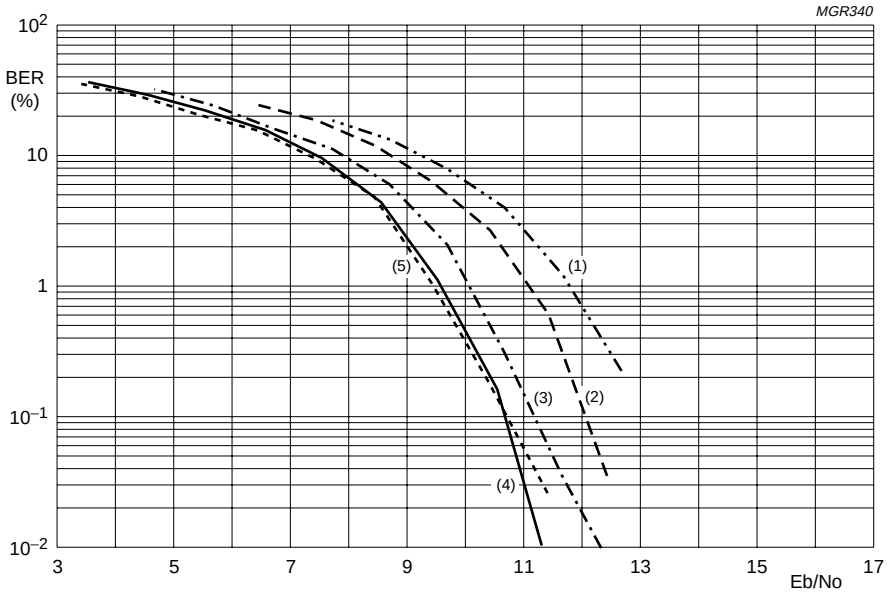
Table 37 Offset coding (2s complement)

OFFSET (Hz)	CODE (AVG6 TO AVG0)
−9450	0111111
−9300	0111110
...	...
−300	0000010
−150	0000001
0	0000000
150	1111111
300	1111110
...	...
9300	1000001
9450	1000000



(1) 2 level 1200.
(2) 2 level 1600.
(3) 2 level 3125.
(4) 2 level 2400.
(5) 2 level 3200.

Fig.24 Demodulator performance in 2L mode.



(1) 4 level 1200.
(2) 4 level 1600.
(3) 4 level 3125.
(4) 4 level 2400.
(5) 4 level 3200.

Fig.25 Demodulator performance in 4L mode.

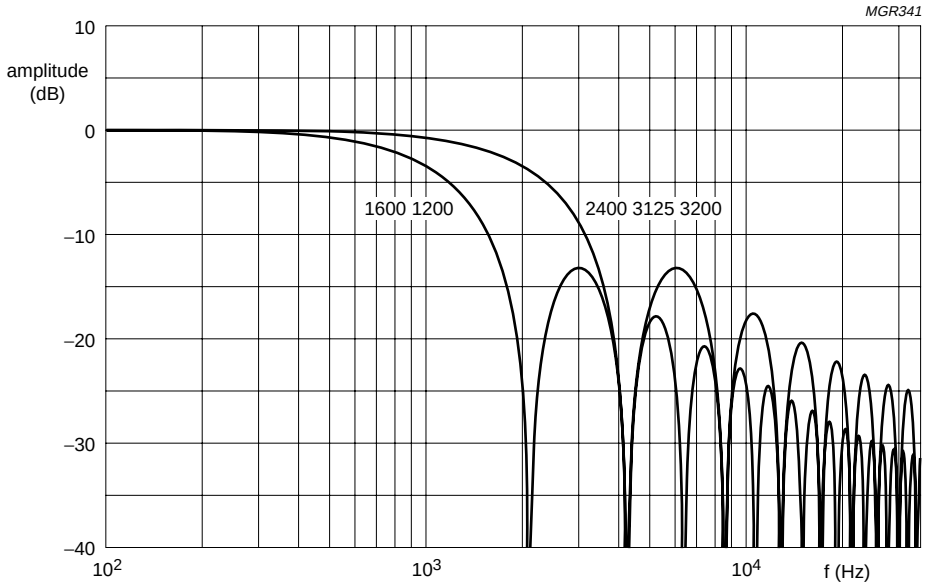


Fig.26 Filter characteristics in direct filter mode.

6.17.1.2 Clock recovery

The clock recovery regenerates the synchronization clock using the edges of the incoming NRZ data. When the NRZ data have no edges for a long time, the synchronization is maintained by means of the correction information from the clock correction block.

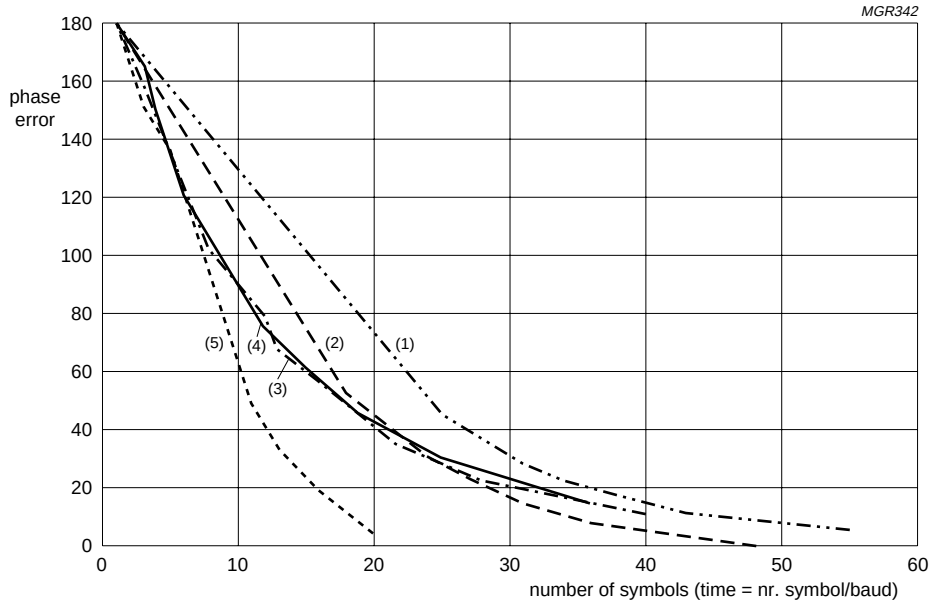
While the clock recovery is disabled, the momentary phase of the recovered clock is frozen. If the clock recovery is enabled at the same relative position within one bit, where it was disabled, then the recovered clock phase will be correct immediately.

The recovered clock is used to sample and shift to left into an internal register one bit each symbol period in 2-FSK and two bits in 4-FSK. The symbol period is determined by bits BD2 to BD0. On the basis of BD bits the demodulator filter length is also set.

In the clock recovery, a pulse (SYMCLK) is generated each n-bits, where n is defined by means of bits B2 to B0. This pulse is used to update the register DMD3. Moreover, it can be used as interrupt to the processor through the IRQ1.3 (symbol interrupt).

The interrupt informs the controller that n bits are available in the register DMD3.

The worst case time required to synchronize to incoming data, when completely out of phase, is plotted for the different baud rates in the following figure (see Fig.27).



(1) 2 level 1200.
(2) 2 level 1600.
(3) 2 level 3125.
(4) 2 level 2400.
(5) 2 level 3200.

Fig.27 Transient phase error due to an input signal phase step of 180 degrees for the different baud rates.

6.17.1.3 Baud rate selection

No bits are lost when switching between single and double baud rates as e.g. required for high speed protocol synchronization. Figure 27 shows how the PCA5010 reacts in this situation.

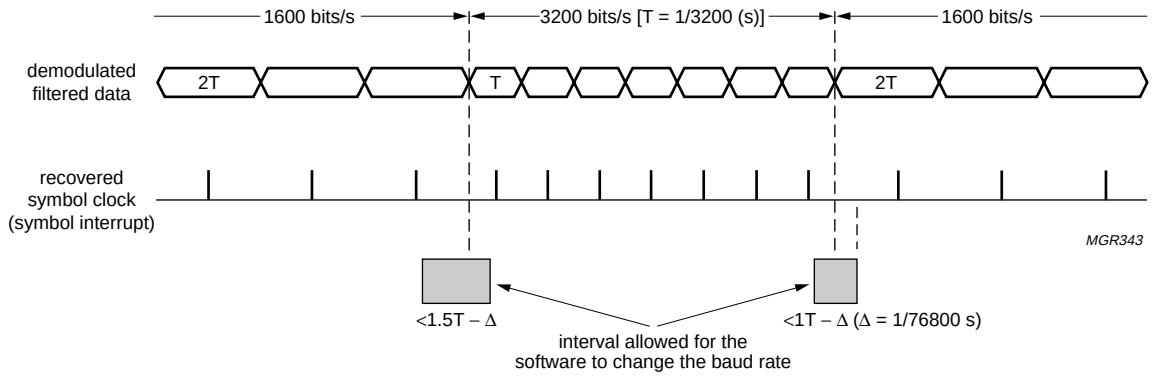


Fig.28 Switching between single and double baud rates (e.g. advanced high speed paging protocol synchronization).

6.17.2 Demodulator Control Register (DMD0)

The demodulator control register DMD0 contains the control bits for enabling the demodulator function and setting its mode and data rate.

Table 38 Demodulator Control Register (DMD0, SFR address ECH)

7	6	5	4	3	2	1	0
ENB	M	–	RES	LEV	BD2	BD1	BD0

Table 39 Description of the DMD0 bits

BIT	SYMBOL	FUNCTION
DMD0.7	ENB	enable demodulator function
DMD0.6	M	mode selection: logic 0 = I/Q from zero-IF receiver, logic 1 = NRZ data
DMD0.5	–	not used
DMD0.4	RES	reserved for future implementation
DMD0.3	LEV	if set to logic 0 2-FSK demodulation, if set to logic 1 4-FSK demodulation
DMD0.2	BD2	baud rate setting; see Table 40
DMD0.1	BD1	
DMD0.0	BD0	

Table 40 Baud rate for bits BD2, BD1 and BD0

BITS			BAUD RATE
BD2	BD1	BD0	
0	0	0	1200 symbols/s
0	0	1	2400 symbols/s
0	1	0	1600 symbols/s
0	1	1	3200 symbols/s
1	0	0	undefined
1	0	1	undefined
1	1	0	undefined
1	1	1	3125 symbols/s

6.17.3 Demodulator averaging Register (DMD1)

The demodulator averaging register DMD1 contains the control bit for enabling the averaging function, used for the offset compensation during demodulation and the coded average (offset) value.

Table 41 Demodulator averaging Register (DMD1, SFR address EDH)

7	6	5	4	3	2	1	0
ENA	AVG6	AVG5	AVG4	AVG3	AVG2	AVG1	AVG0

Table 42 Description of the DMD1 bits

BIT	SYMBOL	FUNCTION
DMD1.7	ENA	enable averaging function/offset calculation
DMD1.6	AVG6	7-bit value indicating the offset value of the demodulator. This is an indication of the LO offset frequency and will be used to determine the AFC output voltage. For coding see Table 37.
DMD1.5	AVG5	
DMD1.4	AVG4	
DMD1.3	AVG3	
DMD1.2	AVG2	
DMD1.1	AVG1	
DMD1.0	AVG0	

6.17.4 Clock Recovery Control Register (DMD2)

The clock recovery control register DMD2 contains the control bits for enabling the clock recovery function and setting its mode.

Whenever the clock recovery function is enabled (DMD2.7 = 1) the positive edge of the synchronized SYMCLK signal will force a SymClk interrupt through the IRQ1.3 request flag after [B2, B1 and B0] received bits (see Table 50).

Table 43 Clock Recovery Control Register (DMD2, SFR address EEH)

7	6	5	4	3	2	1	0
ENC	–	BF	–	TEST	B2	B1	B0

Table 44 Description of the DMD2 bits

BIT	SYMBOL	FUNCTION
DMD2.7	ENC	enable clock recovery function
DMD2.6	–	not used
DMD2.5	BF	bypass demodulator filter
DMD2.4	–	not used
DMD2.3	TEST	reserved, should always be logic 0
DMD2.2	B2	select number of bits per interrupt: If LEV = 0 then 000 = 1-bit, 001 = 2-bit to 111 = 8-bit If LEV = 1 then 00X = 2-bit, 01X = 4-bit, 10X = 6-bit, 11X = 8-bit
DMD2.1	B1	
DMD2.0	B0	

6.17.5 Demodulator Data Register (DMD3)

The demodulator data register DMD3 contains the (demodulated) recovered received symbols.

Table 45 Demodulator Data Register (DMD3, SFR address EFH)

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Table 46 Description of DMD3 bits

BIT	SYMBOL	FUNCTION
DMD3.7	D7	Recovered symbols. The number of relevant bits is set with DMD2[2 to 0].
DMD3.6	D6	
DMD3.5	D5	
DMD3.4	D4	
DMD3.3	D3	
DMD3.2	D2	
DMD3.1	D1	
DMD3.0	D0	

6.18 AFC-DAC

6.18.1 FUNCTION

The AFC digital-to-analog converter provides an analog signal to the receiver to reduce its frequency offset. The analog signal is available at pin 18 (AFCOUT).

For low noise sensitivity the DAC output is buffered and can drive a load impedance of 10 kΩ (max.). The output swing is from rail-to-rail V_{DD}. When the enable signal ENB is at logic 1 a linear binary conversion is performed according to Table 47.

Below 0.2 V the linearity of the output voltage is not ideal.

When ENB is logic 0 the AFCOUT pin is tied to V_{SS} and all currents are switched off.

Table 47 Coding of AFC-DAC

CODE	OUTPUT VOLTAGE
000000	0
000001	$1 \times 1/64 V_{DD}$
...	...
N	$N \times 1/64 V_{DD}$
...	...
111111	$63 \times 1/64 V_{DD}$

6.18.2 AFC-DAC CONTROL/DATA REGISTER (AFCON)

The AFC-DAC Control/Data register AFCON contains the control bit for enabling the AFC-DAC and the data bits for setting the output voltage.

Table 48 AFC-DAC Control/Data Register (AFCON, SFR address 9EH)

7	6	5	4	3	2	1	0
ENB	–	AFC5	AFC4	AFC3	AFC2	AFC1	AFC0

Table 49 Description of the AFCON bits

BIT	SYMBOL	FUNCTION
AFCON.7	ENB	Enable DAC output.
AFCON.6	–	Not used.
AFCON.5	AFC5	6-bit value for DAC output according to Table 47.
AFCON.4	AFC4	
AFCON.3	AFC3	
AFCON.2	AFC2	
AFCON.1	AFC1	
AFCON.0	AFC0	

6.19 Interrupt system

External events and the real-time-driven on-chip peripherals require service by the CPU asynchronously to the execution of any particular section of code. To tie the asynchronous activities of these functions to normal program execution a multiple-source, two-priority-level, nested interrupt system is provided. The interrupt system is shown in Fig.34. The PCA5010 acknowledges interrupt requests from fifteen sources as follows:

- INT0 to INT4 and INT6
- Timer 0 and Timer 1
- Wake-up counter
- I^2C-bus serial I/O
- UART transmitter and receiver
- Demodulator
- DC/DC converter
- Watchdog timer
- Real-time clock (MINUTE).

Each interrupt vectors to a separate location in program memory for its service routine. Each source can be individually enabled or disabled by its corresponding bit in the Interrupt Enable Registers (IEN0 and IEN1).

The priority level is selected via the Interrupt Priority Registers (IP0 and IP1). All enabled sources can be globally disabled or enabled.

6.19.1 Overview

The interrupt controller implemented in the PCA5010 has 15 interrupt sources, of which some are level sensitive and some are edge sensitive. The interrupt controller samples all active sources during one instruction cycle. Evaluation of the interrupts is then performed. A priority decoder decides which interrupt is serviced. Each interrupt has its own vector pointing to an 8 bytes long program segment. A low priority interrupt can be interrupted by a high priority interrupt, but not by another low priority interrupt i.e. only two interrupt levels are possible. Between the RETI instruction (Return from Interrupt) and the LCALL to a next interrupt vector at least one instruction of the lower program level is executed (see Fig.29).

An interrupt is performed with a long subroutine call (LCALL) to vector address, which is determined by the respective interrupt. During LCALL the PC is pushed onto the stack. Returning from interrupt with RETI, the PC is popped from the stack.

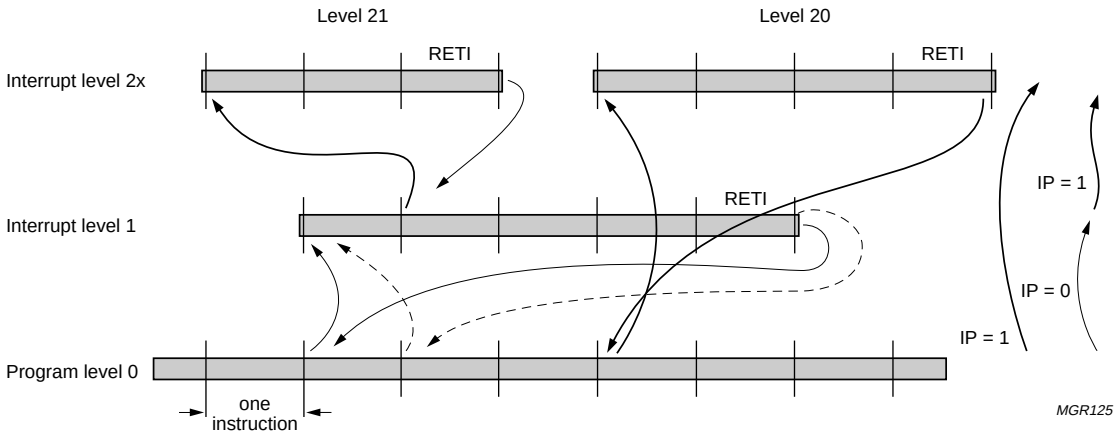


Fig.29 Interrupt hierarchy.

6.19.2 INTERRUPT PROCESS

Sample the interrupt lines: The interrupt lines are latched at the beginning of each instruction cycle.

Analyse the requests: The sampled interrupt lines will be analysed with respect to the relevant Interrupt Enable register (IEx) and Interrupt Priority register (IPx).
The process will deliver the vector of the highest interrupt request and the priority information. Depending on the interrupt level and the priority of the interrupt in progress, an interrupt request to the core is performed. The vector address will be passed to the core process.

Interrupt request to core:

Level 0: The interrupt request to the core is performed, when at least one instruction is performed since the RETI from Level 1.

Level 1: The interrupt request is performed, when at least one instruction is performed since the RETI from Level 21 and the request has high priority.

Level 20: No request is performed.

Level 21: No request is performed.

Emulation: In break mode no interrupt request is performed.

Update the interrupt level:

Level 0: In the event of a high priority interrupt the new level will be Level 20. If it is a low priority interrupt, the new level will be Level 1.

Level 1: In the event of a high priority interrupt, the new level will be Level 21. A low priority interrupt is not performed, the level is unchanged. On RETI the new level will be Level 0.

Level 20: On RETI, the new level is Level 0.

Level 21: On RETI, the new level is Level 1.

Level 1: On RETI, the new level is Level 0.

Level 0: The new level is Level 0.

Clearing the flags: During the forced LCALL the interrupt flag of the relevant interrupt is cleared by hardware, if applicable, otherwise by software.

Emulation: During emulation the interrupts may be disabled. This is performed during break mode. With $\overline{INTD}$ asserted, all the interrupts are disabled.

Idle and power-down: When Idle (PCON.0) or power-down (PCON.1) is set, the interrupt controller waits for the according WUI signal. Because the interrupt controller is waiting for WUI, all activity in the circuit will be stopped, thus no handshake can be completed. The WUI signal for Idle is the OR of all the interrupt request bits and the reset. For power-down the WUI signal is built only with the Port 1 interrupt request flags and the reset.

6.19.3 INTERRUPT CONTROLLER RELATED SFRS

The implementation of the interrupt controller related SFRs for enabling and disabling interrupts is identical to a standard 80C51, but the interrupt sources have been changed according to Table 50.

Table 50 Interrupt controller related SFRs: IEN0 (A8H), IEN1 (E8H), IP0 (B8H), IP1 (F8H), IRQ1 (C0H), TCON (88H), WUCON (94H) and RTCON (CDH)

BITS	CONV. NAME	SOURCE	NOTES
IEN0 address A8H: interrupt enable for X0, X1, T0, T1, T2, S0, S1 and global interrupt enable			
0	EX0	P3.2	Enables or disables EXTERNAL0 interrupt. If EX0 = 0, the external interrupt 0 is disabled.
1	ET0	TIMER0	Enables or disables the TIMER 0 overflow interrupt. If ET0 = 0, the Timer 0 interrupt is disabled.
2	EX1	P3.3	Enables or disables the EXTERNAL1 interrupt. If EX1 = 0, external interrupt 1 is disabled.
3	ET1	TIMER1	Enables or disables TIMER 1 overflow interrupt. If ET1 = 0, the Timer 1 interrupt is disabled.
4	ES0	UART	Enables or disables the UART interrupt. If ES0 = 0, the UART interrupt is disabled.
5	ES1	I^2C	Enables or disables the I^2C-bus interrupt. If ES1 = 0, the I^2C-bus interrupt is disabled.
6	ET2	WAKE-UP	Enables or disables the WAKE-UP interrupt. If ET2 = 0, the WAKE-UP interrupt is disabled.
7	EA	/	Disables all interrupts. If EA = 0, no interrupt will be acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
IEN1 address E8H: interrupt enable for X2 to X9			
0	EX2	P1.0	Enables or disables interrupts on P1.0. If EX2 = 0, the corresponding interrupt is disabled.
1	EX3	P1.1	Enables or disables interrupts on P1.1. If EX3 = 0, the corresponding interrupt is disabled.
2	EX4	P1.2	Enables or disables interrupts on P1.2. If EX4 = 0, the corresponding interrupt is disabled.
3	EX5	SYMBOL	Enables or disables the SYMBOL interrupt. If EX5 = 0, the SYMBOL interrupt is disabled.
4	EX6	P1.4	Enables or disables interrupts on P1.4. If EX6 = 0, the corresponding interrupt is disabled.
5	EX7	DC/DC	Enables or disables the DC/DC converter interrupt. If EX7 = 0, the DC/DC converter interrupt is disabled.
6	EX8	WDI	Enables or disables interrupts on the watchdog. If EX8 = 0, the WDINT interrupt is disabled.
7	EX9	MIN	Enables or disables real-time clock interrupt. If EX9 = 0, the MINUTE interrupt is disabled.
IP0 address B8H: interrupt priority for X0, X1, T0, T1, S0 and S1			
0	PX0	P3.2	Defines the EXTERNAL0 interrupt 0 priority level. PX0 = 1 programs it to the higher priority level.
1	PT0	TIMER0	Enables or disables the TIMER 0 interrupt priority level. PT0 = 1 programs it to the higher priority level.
2	PX1	P3.3	Defines the EXTERNAL1 interrupt priority level. PX1 = 1 programs it to the higher priority level.
3	PT1	TIMER1	Defines the TIMER 1 interrupt priority level. PT1 = 1 programs it to the higher priority level.

BITS	CONV. NAME	SOURCE	NOTES
4	PS0	UART	Defines the UART interrupt priority level. PS0 = 1 programs it to the higher priority level.
5	PS1	I^2C	Defines the I^2C-bus interrupt priority level. PS1 = 1 programs it to the higher priority level.
6	PT2	WAKE-UP	Defines the WAKE-UP interrupt priority level. PT2 = 1 programs it to the higher priority level.
7	–	/	Unused.
IP1 address F8H: interrupt priority for X2 to X9			
0	PX2	P1.0	Defines the EXTERNAL2 interrupt priority level 1. PX2 = 1 programs it to the higher priority level.
1	PX3	P1.1	Defines the EXTERNAL3 interrupt priority level 1. PX3 = 1 programs it to the higher priority level.
2	PX4	P1.2	Defines the EXTERNAL4 interrupt priority level 1. PX4 = 1 programs it to the higher priority level.
3	PX5	SYMBOL	Defines the SYMBOL interrupt priority level 1. PX5 = 1 programs it to the higher priority level.
4	PX6	P1.4	Defines the EXTERNAL6 interrupt priority level 1. PX6 = 1 programs it to the higher priority level.
5	PX7	DC/DC	Defines the DC/DC converter interrupt priority level 1. PX7 = 1 programs it to the higher priority level.
6	PX8	WDI	Defines the WATCHDOG interrupt priority level 1. PX8 = 1 programs it to the higher priority level.
7	PX9	MIN	Defines the REAL-TIME CLOCK interrupt priority level 1. PX9 = 1 programs it to the higher priority level.
TCON address 88H: timer/counter mode control register			
0	IT0	P3.2	EXTERNAL0 interrupt type control bit. Set/cleared by software to specify falling edge/low level triggered external interrupt.
1	IE0	P3.2	EXTERNAL0 interrupt flag. Set by hardware when external interrupt detected. Cleared by hardware.
2	IT1	P3.3	EXTERNAL1 interrupt type control bit. Set/cleared by software to specify falling edge/low level triggered external interrupt.
3	IE1	P3.3	EXTERNAL1 interrupt flag. Set by hardware when external interrupt detected. Cleared by hardware.
4	TR0	TIMER0	TIMER 0 run control bit. Set/cleared by software to turn timer on/off.
5	TF0	TIMER0	TIMER 0 overflow flag. Set by hardware on timer/counter overflow. Cleared by hard or software.
6	TR1	TIMER1	TIMER 1 run control bit. Set/cleared by software to turn timer on/off.
7	TF1	TIMER1	TIMER 1 overflow flag. Set by hardware on timer/counter overflow. Cleared by hard or software.
IRQ1 address C0H: interrupt request register for X2 to X9			
0	IQ2	P1.0	Interrupt request flag from P1.0.
1	IQ3	P1.1	Interrupt request flag from P1.1.
2	IQ4	P1.2	Interrupt request flag from P1.2.

BITS	CONV. NAME	SOURCE	NOTES
3	IQ5	SYMBOL	Interrupt request flag from clock recovery circuit. Set by hardware or software. Cleared by software.
4	IQ6	P1.4	Interrupt request flag from P1.4.
5	IQ7	DC/DC	Interrupt request flag from DC/DC-CONVERTER. Set by hardware or software. Cleared by software.
6	IQ8	WDI	Interrupt request flag from watchdog timer. Set by hardware or software. Cleared by software.
7	IQ9	MIN	Interrupt request flag from real-time clock interrupt. Set by hardware or software. Cleared by software.
WUCON address 94H: wake-up counter control register			
0	SET	–	Latch signal to copy content of WUC to peripheral register.
1	LOAD	–	Parallel load signal for wake-up counter.
2	Z0	–	
3	Z1	–	
4	CPL	–	Complete interrupt flag from wake-up counter timer. Set by hardware or software. Cleared by software.
5	unused	–	
6	WUP	–	WUP interrupt flag from wake-up counter timer. Set by hardware or software. Cleared by software.
7	RUN	–	RUN bit for wake-up counter.
RTCON address CDH: real-time clock control register			
0	SET	–	Latch signal to copy content of WUC to peripheral register.
1	LOAD	–	Load RTC0 value from SFR to RTC.
2	W/$\overline{R}$	–	Disable write back to SFR.
3 to 6	unused	–	
7	MIN	–	Interrupt request flag from RTC. Set by hardware or software. Cleared by software.

Notes

1. IEN0 and IEN1: These are two 8-bit registers that control the enabling of the 15 interrupt sources individually as well as a global enable/disable for all of the sources.
2. IP0 and IP1: These are two 8-bit registers that set priority for each interrupt source. IP0 actually contains only 7 bits as IP.7 is not implemented. This bit will always read as logic 0.

6.19.4 PORT 3 INTERRUPTS: P3.2 AND P3.3

INT0 and INT1 are level or edge sensitive.
The programming is performed with TCON. Since P3.2 and P3.3 are configured as push-pull outputs, these interrupts can only be triggered by output commands to these ports and not by external events.

TCON.0 (IT0): Interrupt 0 type control bit. Set/cleared by software to specify falling edge/low level triggered external interrupt (see Fig.30).

TCON.1 (IE0): Interrupt 0 flag. Set by hardware when an external interrupt is detected. Cleared by hardware when the service routine is called.

TCON.2 (IT1): Interrupt 1 type control bit. Set/cleared by software to specify falling edge/low level triggered external interrupt.

TCON.3 (IE1): Interrupt 0 flag. Set by hardware when an external interrupt is detected. Cleared by hardware when the service routine is called.

6.19.5 WAKE-UP INTERRUPT

The wake-up interrupt (T2) is the level sensitive OR-function of WUP bit or CPL bit in the WUCON SFR. The wake-up interrupt is mapped to the T2 vector (see Fig.30). These flags are set by hardware and need to be cleared by software. For more information see Section 6.14.

WUCON.6 (WUP): WUP interrupt flag. Attention: writing and reading this SFR bit does not access the same flag. The flag is set by hardware and needs to be cleared by software.

WUCON.4 (CPL): Complete flag. The previous set instruction is completed. The settings of the SFR have been copied to the peripheral block. The flag is set by hardware and needs to be cleared by software.

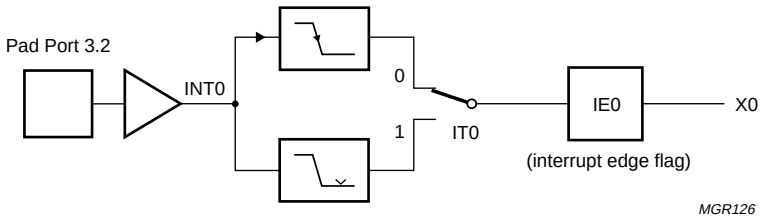


Fig.30 External interrupt Port 3.2 and Port 3.3 (INT0 and INT1).

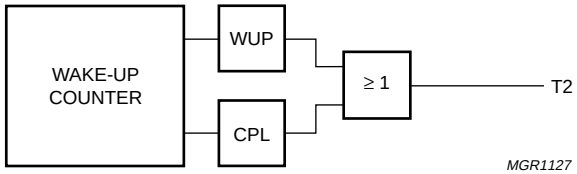


Fig.31 Wake-up interrupt.

6.19.6 PORT 1 INTERRUPTS: PORT 1.0 TO PORT 1.4 (INT2 TO INT6)

Four Port 1 lines can be used as external interrupt inputs (see Fig.30). When enabled (IEN1 SFR), each of these lines may wake-up the device from power-down. Using the IX1 register, each of these port lines may be set active to either HIGH or LOW. IRQ1 is the interrupt request flag register. Each flag, if the interrupt is enabled, will send an interrupt request, but must be cleared by software, i.e. via the interrupt software. The Port 1 interrupt request flags can only be set if the corresponding interrupt enable bit is set.

6.19.7 MORE INTERRUPTS: SYMCLK, DC/DC, WATCHDOG AND MINUTE

The decoder blocks generate events that can force an interrupt when enabled (IEN0 and IEN1 SFR). These interrupts are mapped to the corresponding P1 interrupt request flag register bits (see Fig.33). Each flag, if the interrupt is enabled, will send an interrupt request and must be cleared by software, i.e. via the interrupt service routine.

The IRQ bits are not set if the corresponding enable is not set.

IRQ1.3: (symbol interrupt): this interrupt request flag, if enabled, is set if the demodulator (clock recovery) has data ready, that should be read by the microcontroller. The event is called symbol clock or SymClk, because in one mode of operation one symbol is delivered per interrupt. The flag is set by hardware and needs to be cleared by software.

IRQ1.5: (DC/DC converter interrupt); this interrupt request flag, if enabled, is set if the DC/DC converter is not able to deliver the required current (STB flag cleared). The flag is set by hardware and needs to be cleared by software.

IRQ1.6: (watchdog interrupt); this interrupt request flag, if enabled, is set if the watchdog timer will expire within $^{1}/_{16}$ s. The flag is set by hardware and needs to be cleared by software.

IRQ1.7: (minute interrupt). This interrupt request flag, if enabled, is set each minute once by the real-time clock. The flag is set by hardware and needs to be cleared by software.

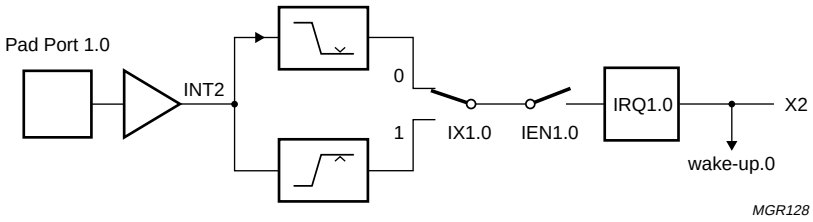


Fig.32 Interrupt Port 1.0.

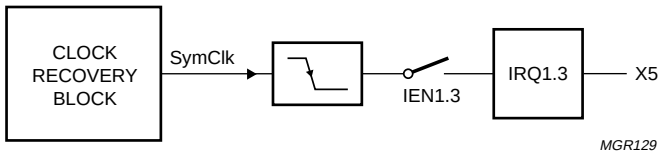


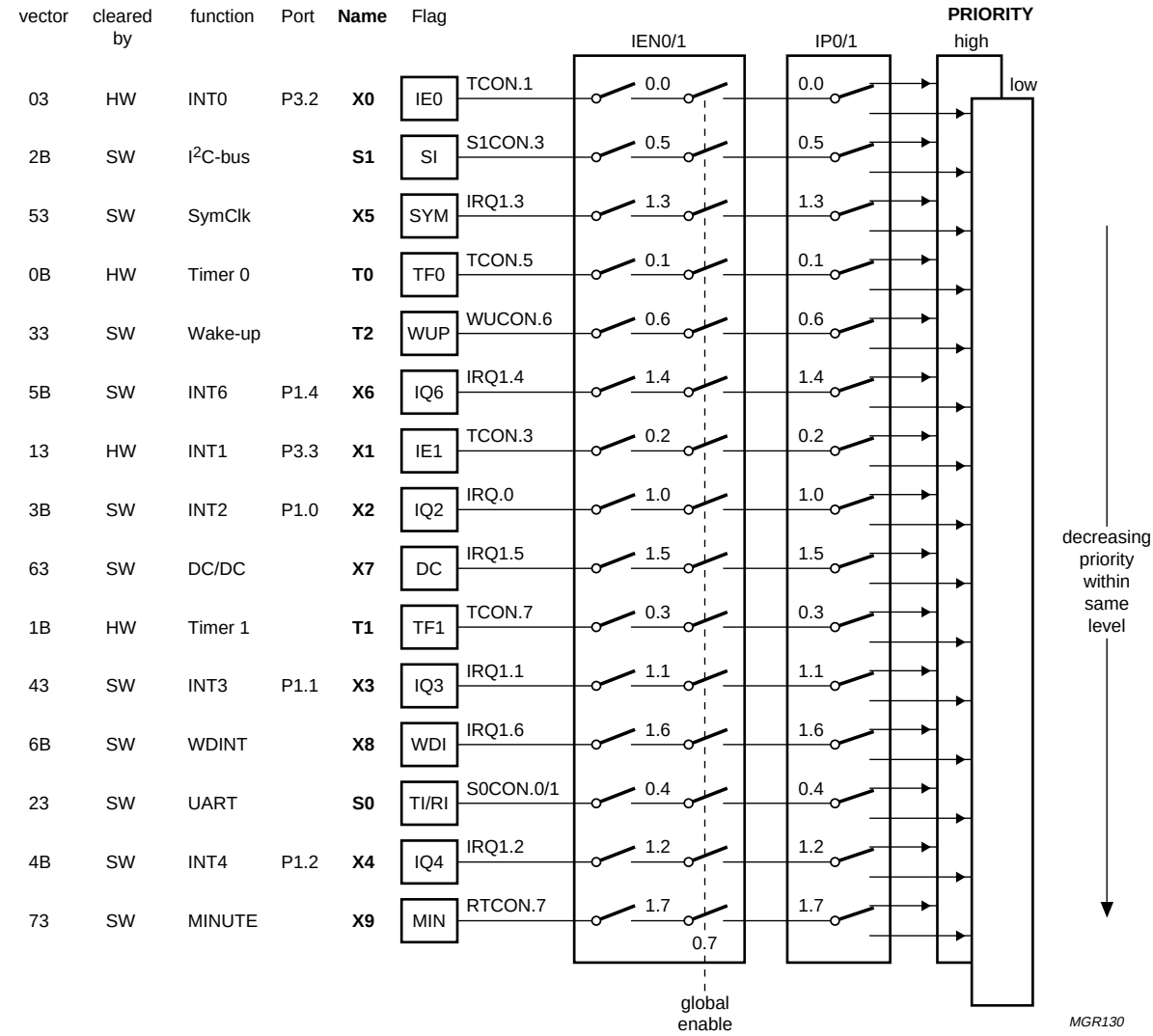
Fig.33 SymClk (as example for any of the 4 mentioned interrupts).

6.19.8 INTERRUPT HANDLING

Figure 34 shows the conventions for interrupt assignments and priorities.

Arbitration of several simultaneously sampled interrupts can be seen from Fig.34. The sampled interrupt with the highest priority will be handled first (assuming that the Interrupt Priority is default).

Setting of interrupt request flags for X2 to X9 is masked by the corresponding interrupt enable bit (IEN1).


vector
cleared by
function
Port
Name
Flag
IEN0/1
IP0/1
PRIORITY
high
low
03 HW INT0 P3.2 X0 IE0 TCON.1 0.0 0.0
2B SW I2C-bus S1 SI S1CON.3 0.5 0.5
53 SW SymClk X5 SYM IRQ1.3 1.3 1.3
0B HW Timer 0 T0 TF0 TCON.5 0.1 0.1
33 SW Wake-up T2 WUP WUCON.6 0.6 0.6
5B SW INT6 P1.4 X6 IQ6 IRQ1.4 1.4 1.4
13 HW INT1 P3.3 X1 IE1 TCON.3 0.2 0.2
3B SW INT2 P1.0 X2 IQ2 IRQ.0 1.0 1.0
63 SW DC/DC X7 DC IRQ1.5 1.5 1.5
1B HW Timer 1 T1 TF1 TCON.7 0.3 0.3
43 SW INT3 P1.1 X3 IQ3 IRQ1.1 1.1 1.1
6B SW WDINT X8 WDI IRQ1.6 1.6 1.6
23 SW UART S0 TI/RI S0CON.0/1 0.4 0.4
4B SW INT4 P1.2 X4 IQ4 IRQ1.2 1.2 1.2
73 SW MINUTE X9 MIN RTCON.7 1.7 1.7
0.7
global enable
decreasing priority within same level
MGR130

Note: The signal level applied to the $\overline{EA}$ pin defines whether the interrupt vector code is fetched from external or internal ROM.

Fig.34 Interrupt assignment and priorities.

6.20 Idle and power-down operation

Idle and power-down are power saving modes of the microcontroller that can be activated when no CPU activity is required. Both modes do not stop the 76.8 kHz oscillator nor disable any peripheral function.

The following functions remain active during the Idle mode:

- Timer 0 and Timer 1
- Wake-up counter
- Watchdog counter
- Real-time clock
- Demodulator and clock recovery
- UART
- I^2C-bus
- External interrupt.

6.20.1 IDLE MODE

The instruction that sets PCON.0 is the last instruction executed in the normal operating mode before the Idle mode is activated. Once in the Idle mode, the CPU status is preserved together with the stack pointer, program counter, program status word and accumulator. The RAM and all other registers maintain their data during Idle mode. The status of the external pins during Idle mode is shown in Table 51.

There are two ways to terminate the Idle mode:

1. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware thus terminating the Idle mode. The interrupt is serviced, and following the RETI instruction, the next instruction to be executed will be the one following the instruction that put the device in the Idle mode. The flag bits GF0 and GF1 may be used to determine whether the interrupt was received during normal execution or during the Idle mode. For example, the instruction that writes to PCON.0 can also set or clear one or both flag bits. When the Idle mode is terminated by an interrupt, the service routine can examine the status of the flag bits.
2. The second way of terminating the Idle mode is with an internal or external hardware reset. Reset redefines all SFRs but does not affect the on-chip RAM. Possible sources of an internal reset are
   a) Watchdog reset if the watchdog had expired
   b) Off/on reset if the DC/DC converter is restarted from off mode (wake-up counter, RTC or P1 pins).

6.20.2 POWER-DOWN MODE

The instruction that sets PCON.1 is the last instruction executed in the normal operating mode before the power-down mode is activated. Once in the power-down mode, the CPU status is preserved together with the stack pointer, program counter, program status word and accumulator. The RAM and all other registers maintain their data during power-down mode. The status of the external pins during power-down mode is shown in Table 51.

There are two ways to terminate the power-down mode:

1. Activation of an enabled external interrupt [INT2 to INT9] will cause PCON.1 to be cleared by hardware thus terminating the power-down mode. The interrupt is serviced, and following the RETI instruction, the next instruction to be executed will be the one following the instruction that put the device in the power-down mode.
2. The second way of terminating the power-down mode is with an internal or external hardware reset. Reset redefines all SFRs but does not affect the on-chip RAM. Possible sources of an internal reset are
   a) Watchdog reset if the watchdog had expired
   b) Off/on reset if the DC/DC converter is restarted from off mode (wake-up counter or P1 pins).

The power-down mode is not specially useful. It has been implemented for compatibility only. The Idle mode has the same power saving capability and allows much more flexible wake-up.

6.20.3 OFF MODE

The off mode has been designed as the power saving mode of the PCA5010. Shortly after entering this mode the DC/DC converter is switched off and V_{DD} is reduced to V_{BAT}. Directly after activating the off mode, the CPU must be set in Idle mode.

The off mode is entered by:

1. ORL DCCON0, #80H
2. ORL PCON, #01H.

The off mode can be exited by one of the following events:

- RTC minute event
- Wake-up counter event
- Event on any P1 pin
- RESETIN active HIGH.

Each of these events first starts the DC/DC converter to ramp up V_{DD} to 2.2 V. After an initial reset, generated by the DC/DC converter when V_{DD} is again at normal level, all 2 V blocks will restart their operation. The first instruction will be fetched from address 0.

The edge sensitive interrupts (minute and wake-up) from the internal sources have been lost during restart and must be polled from their SFRs. Events from P1 pins can be served after enabling the interrupts, since they are level sensitive.

6.20.4 Status of external pins

The status of the external pins during Idle and power-down mode is shown in Table 51.

Table 51 Status of external pins during normal, Idle and power-down modes

MODE	MEMORY	ALE	$\overline{\text{PSEN}}$	PORT 0	PORT 1	PORT 2	PORT 3
Normal	internal	0	1	port data	port data	port data	port data
Idle	internal	1	1	port data	port data	port data	port data
	external	1	1	pull-up HIGH	port data	address	port data
Power-down	internal	0	0	pull-up HIGH	port data	port data	port data
	external	0	0	pull-up HIGH	port data	address	port data

6.20.5 Power Control Register (PCON)

The reduced power modes are activated by software using this special function register. PCON is not bit addressable.

Table 52 Power Control Register (PCON and SFR address 87H)

7	6	5	4	3	2	1	0
SMOD	XRE	ENIS	–	GF1	GF0	PD	IDL

Table 53 Power Control Register (PCON, SFR address 87H)

BIT	SYMBOL	FUNCTION
PCON.7	SMOD	Control bit to double data rate of UART, when set to logic 1.
PCON.6	XRE	If set to logic 1 enables external XRAM from address 0 on, if set to logic 0 the first 1024 XRAM bytes are in internal XRAM, the higher addresses come from external XRAM; see note 1.
PCON.5	ENIS	**Enable ISYNC**. If bit is set, ISYNC can be monitored at pin $\overline{\text{EA}}$ in internal access mode. The binary value of ISYNC changes each time a new instruction is fetched from memory. This bit must not be set to logic 1 by user program!
PCON.4	–	Reserved.
PCON.3	GF1	**General purpose flag bit**.
PCON.2	GF0	**General purpose flag bit**.
PCON.1	PD	**Power-down bit**. Setting this bit activates the power-down mode; see note 2.
PCON.0	IDL	**Idle mode bit**. Setting this bit activates the Idle mode; see note 2.

Notes

1. This device does not support external XRAM access. Therefore the XRE bit is meaningless and should never be written to logic 1.

2. If logic 1s are written to PD and IDL at the same time, PD takes precedence. The reset value of PCON is (00000000).

6.21 Reset

To initialize the PCA5010 a reset is performed by either of 2 methods:

- Applying an external reset signal to the RESETIN pin
- Via the on-chip watchdog timer.

The reset state of the output pins is given in separate tables (Tables 2 to 6). The reset state of SFRs is given in a separate overview (see Table 1).

While a reset is applied to the device the output $\overline{\text{RESOUT}}$ is driven LOW.

The internal RAM is not affected by reset. When V_{DD} is turned on, the RAM contents are indeterminate.

6.21.1 External reset using the RESETIN pin

The external reset input for the PCA5010 is the RESETIN pin. A Schmitt trigger is used at the input for noise rejection. Immediately after the RESETIN goes HIGH, an internal reset is executed. As a consequence the SFRs and port pins adopt their reset state, ALE and $\overline{\text{PSEN}}$ are held HIGH. As long as RESETIN pin stays HIGH, the reset state is maintained. When RESETIN goes LOW, the device start-up sequence is executed (see Section 6.22).

6.21.2 External power-on reset using the RESETIN pin

An automatic reset can be obtained by connecting the RESETIN pin to V_{BAT} via a capacitor and to V_{SS} via a resistor. At power-on, the voltage on the RESETIN pin is equal to V_{BAT} and decreases from V_{BAT} as the capacitor charges through the resistor to V_{SS}. $V_{RESETIN}$ must remain higher than the threshold of the Schmitt trigger for a duration of $t_{RESETIN}$ (see Chapter “AC characteristics”). The reset configuration is shown in Fig.35.

6.21.3 Internal Reset

The watchdog which is available in the PCA5010 (see Section 6.16) will force a reset if it is enabled and expires.

A reset is also forced, when the DC/DC converter restarts operation from off mode (see Section 6.22.3).

All resets to the microcontroller can be observed as negative pulses at the output $\overline{\text{RESOUT}}$.

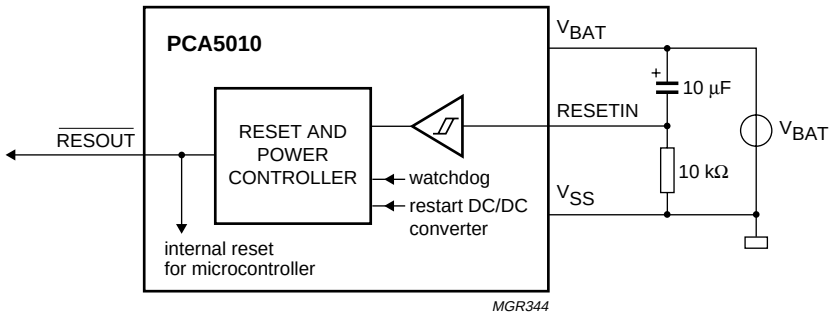


Fig.35 Application diagram for external power-on reset configuration.

6.22 DC/DC converter

6.22.1 FUNCTION

The DC/DC converter converts the voltage from a single primary cell (0.9 to 1.6 V) to a nominal 2.2 V V_{DD} for on-chip and off-chip use. For EMC reasons a special technique is used to minimize coil current ripples under all load conditions.

The voltage generated by the DC/DC converter is available at pin $V_{DD(DC)}$. The supply for all functions of the chip is taken from the V_{DD} and V_{DDA} pins. The user has to connect $V_{DD(DC)}$ to the other V_{DD} pins. The supply used for the reference and comparators is taken from V_{DDA}. A typical circuit configuration is shown in Fig.36.

For a certain current load (I_L) the controller settles to a stable voltage V_{DD} (I_L) in the window 2.15 to 2.25 V. Increasing the load decreases V_{DD} (I_L) by a small amount. When V_{DD} (I_L) drops below 2.15 V the DC/DC converter calculates a new set of coefficients and V_{DD} (I_L) settles again between 2.15 and 2.25 V (see Fig.45).

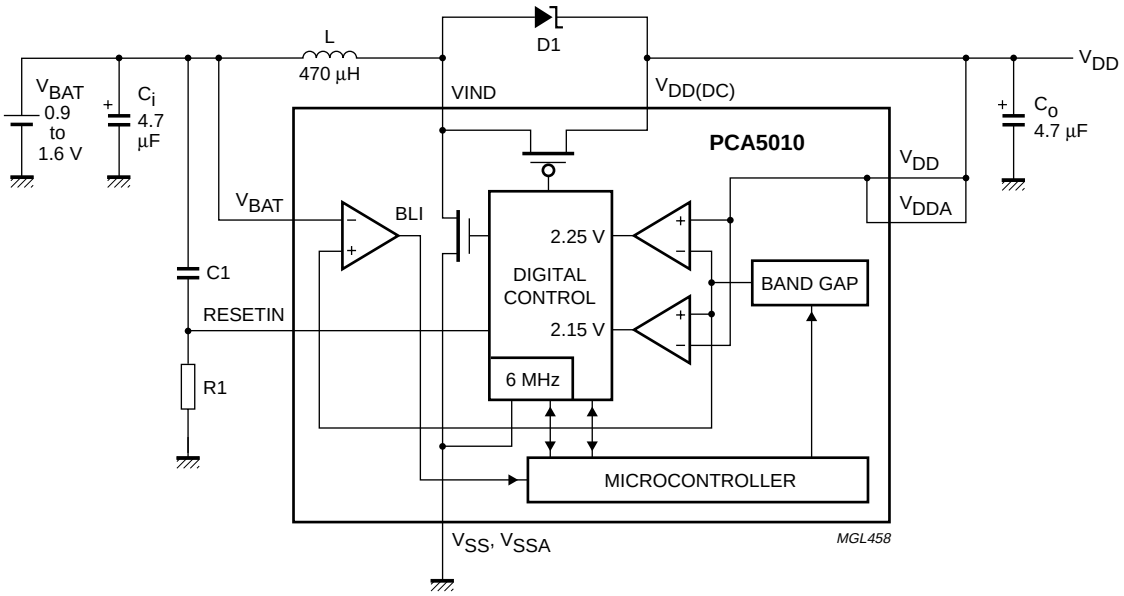


Fig.36 Typical operating circuit.

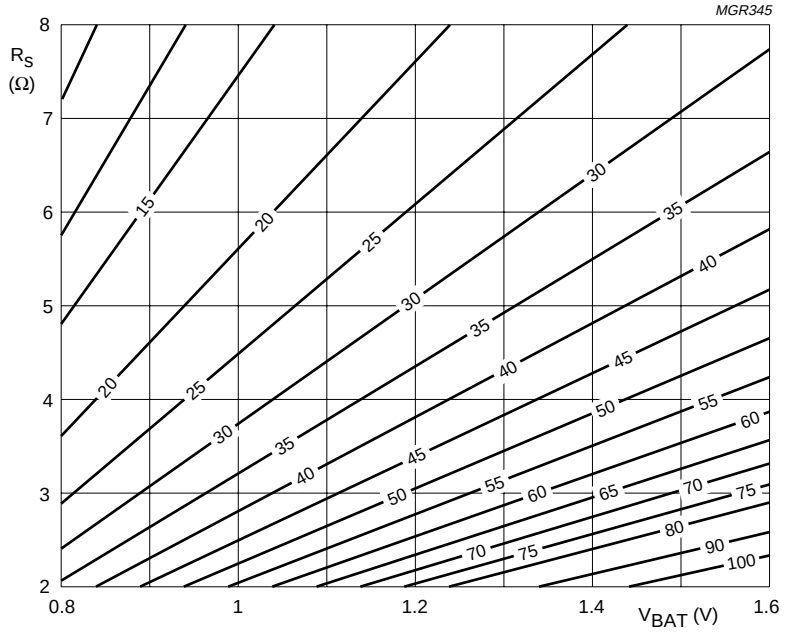
6.22.2 TYPICAL OPERATING CHARACTERISTICS

The maximum power delivered by the DC/DC converter is given by equation (1).

$$P_{o(max)} \leq \frac{(V_{BAT})^2}{4 \cdot R_S} \quad (1)$$

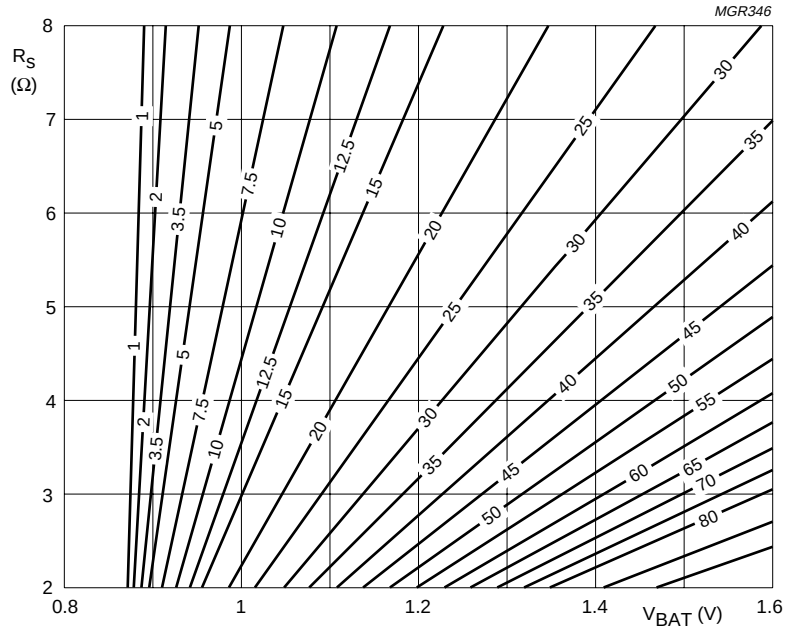
R_S is the total series resistance which is the sum of $R_{BAT} + R_{ind} + R_{sw} + ESR(C_o)$. In Figs 37 and 38 the maximum available output current I_L is shown as a function of V_{BAT} and R_S.

The efficiency is determined by the series resistance R_S and the current consumption of the converter itself. R_S is the sum of the battery resistance R_{BAT}, the DC resistance SRL of the coil, the on resistance of the MOSFET $R_{DS,on}$ and the ESR of the output capacitor C_o. Figure 39a shows the efficiency when using a 470 µH coil with a SRL of 5 Ω and a load capacitor of 4.7 µF with an ESR of 0.5 Ω. In Fig.39b the efficiency for the same configuration is shown but with a SRL of only 0.1 Ω. To increase efficiency for extremely low output currents, the converter should be set into standby mode (see Fig.40).



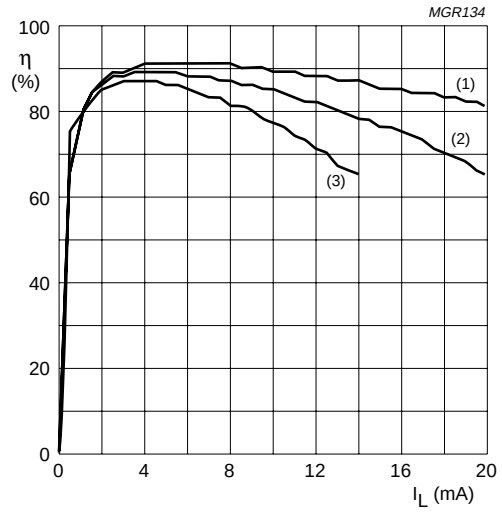
V_{DD} = 2.2 V; $R_S = R_{BAT} + R_{ind} + R_{sw}$.

Fig.37 Maximum available output current (mA) in normal mode.

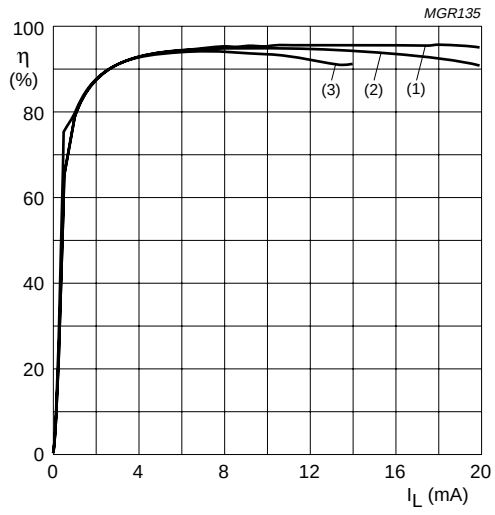


V_{DD} = 2.2 V; $R_s = R_{BAT} + R_{ind} + R_{sw}$.

Fig.38 Maximum available output current (mA) in standby mode.



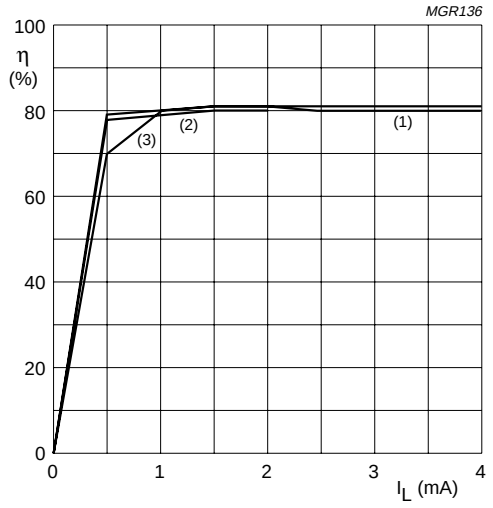
a. R_S = 6 Ω.



b. R_S = 1 Ω.

(1) V_{BAT} = 1.5 V.
(2) V_{BAT} = 1.2 V.
(3) V_{BAT} = 0.9 V.

Fig.39 Efficiency in normal mode as a function of load current.



(1) V_{BAT} = 1.5 V.
(2) V_{BAT} = 1.2 V.
(3) V_{BAT} = 0.9 V.

Fig.40 Efficiency in standby mode as a function of load current.

6.22.3 START-UP DESCRIPTION

6.22.3.1 Start-up from reset

External RC together with an on-chip Schmitt trigger is used to generate a reset pulse after the insertion of a new battery (see Section 6.21). A reset pulse at the RESETIN pin resets the SFRs and the internal registers of the DC/DC converter to the factory programmed values and the start-up sequence shown in Fig.41 is started. The reset pulse must be essentially longer then the rise time of V_{BAT}.

The start-up sequence is divided into several steps:

1. Start-up 76.8 kHz crystal oscillator (256 clocks).
2. Boost up of V_{DD} to approximately 1.7 V using the 76.8 kHz clock. During this phase, the p-channel MOSFET is switched off and the charge is transferred via the external Schottky diode.
3. Start of the 6 MHz clock $\left(2 \times \frac{1}{76.8\ \text{kHz}}\right)$; (see Section 6.12).
4. Boost up V_{DD} to 2.2 V using the internal 6 MHz clock and the p-channel MOSFET. As soon as $V_{DD} \geq 2.15$ V, the stable flag is set to indicate that the system is powered up successfully and the microcontroller starts operation. The DC/DC converter now stays in the normal operating mode.

If a reset pulse is generated during normal operation, the DC/DC converter immediately resets the whole system and enters the start-up sequence.

6.22.3.2 Start-up from off mode

Start-up from off mode behaves exactly as start-up from external reset (see Fig.41) except that:

- The internal registers of the DC/DC converter are not reset; however the DC/DC converter SFRs are reset.

Off mode is exited when one of the following events occur:

- Key pressed
- Minute interrupt
- Wake-up interrupt.

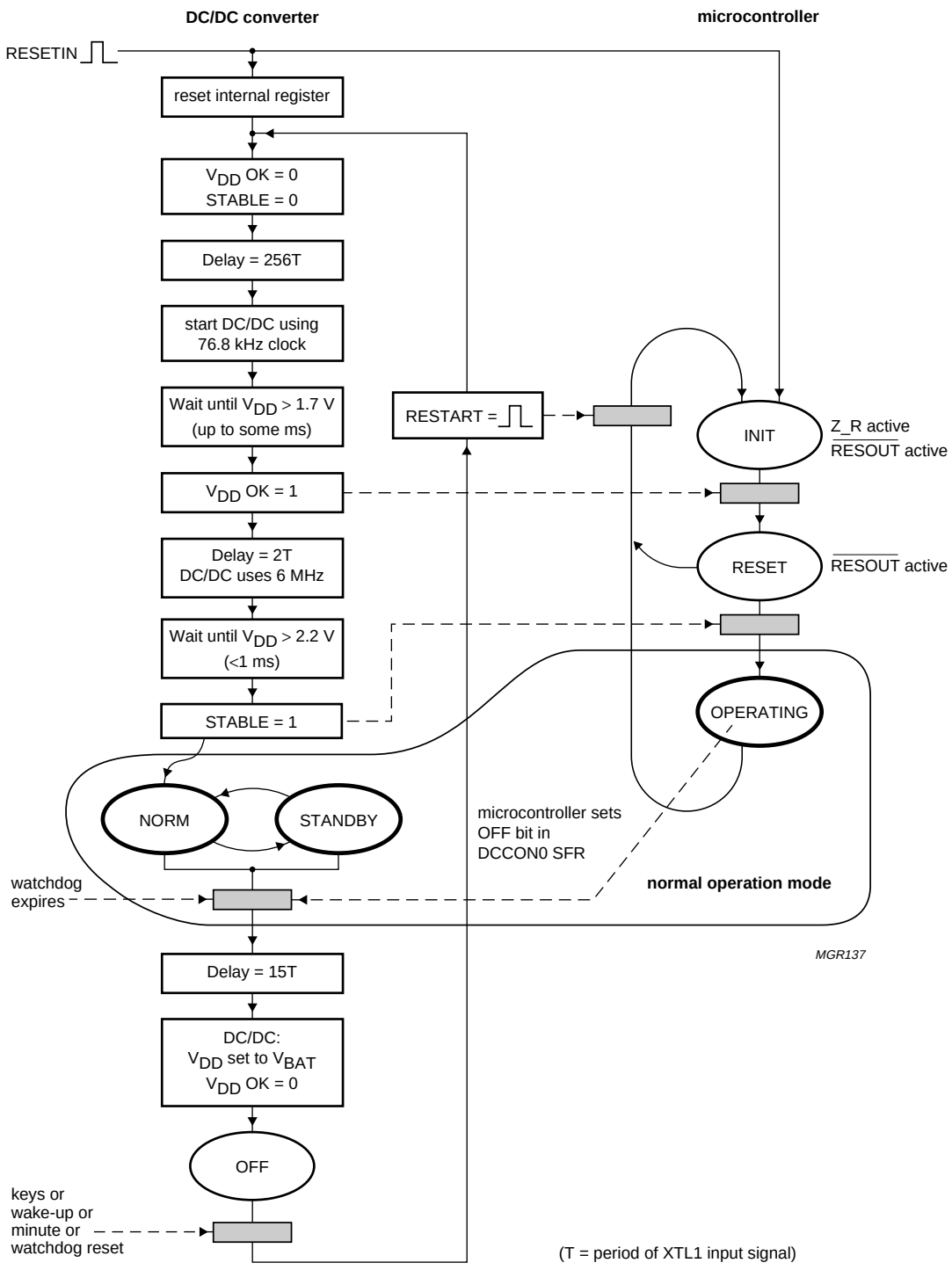


Fig.41 System power-up/off sequencing.

6.22.4 Description of operating modes

6.22.4.1 Normal operating mode

Once the system is powered-up successfully (STB = 1), the DC/DC converter is in normal operating mode. This mode has two sub modes:

- Normal mode
- Standby mode.

By setting/resetting the standby bit in DCCON0 (D1H), the DC/DC converter switches between normal mode and standby mode. Switching between these two modes is possible at any time by software if the controller is in normal operating mode. Normal operating mode can be exited by any of the following events:

- HIGH level at the RESETIN pin
- A watchdog reset, which will force the same sequence as an off command
- Writing the off bit in DCCON0.

Setting the off bit in DCCON0 forces the converter into DC/DC converter off mode.

6.22.4.2 Normal mode

Normal mode is the high efficiency mode of the DC/DC converter. In this mode the controller can keep V_{DD} stable at 2.2 V up to the maximum available current (see Fig.37). The output voltage is regulated in a small window and the current peaks in the coil are kept as small as possible (see Fig.45). After a reset and the following start-up sequence, the controller is in normal mode.

To shorten the settling time when the receiver is switched on or off, the DC/DC converter uses 2 sets of coefficients. One for low output current and one for high output current. When the RXE bit in DCCON0 is set, the DC/DC converter stores the actual coefficients for low output current and switches to the coefficients for high load current. At the same time the receiver should be enabled. When the battery voltage did not change very much since the last time the receiver was on, the settling time is only a few microseconds instead of a few hundreds of microseconds when not using the RXE bit. When switching off the receiver, the RXE bit in DCCON0 should be reset. In this case, the DC/DC converter stores the new values for high output current and restores the values for low output current. It should be noted that the RXE bit does not change the algorithm of the DC/DC converter but shortens the settling time dramatically.

When the load is so high that the required output current cannot be delivered, the DC/DC converter resets the signal STB and a DC/DC interrupt is issued to the processor via IRQ SFR IRQ1.5. STB = 0 flags the inability to deliver enough current in normal mode or in standby mode. When the STB flag is set to logic 0, V_{DD} can drop very quickly, depending on the battery voltage and the load.

6.22.4.3 Standby mode

Standby mode is a low current mode which can be used when only the microcontroller is running and the quality of V_{DD} is not important. In standby mode the DC/DC converter uses the 76.8 kHz clock instead of the 6 MHz clock. This reduces the current consumption of the DC/DC converter. The maximum output current in this mode is limited to a few milliamps (see Fig.38). In standby mode V_{DD} can be set to 1.9, 2.0, 2.1 or 2.2 V by setting the VLO1 and VLO0 bits in DCCON1 to the corresponding values. When the load is so high that the required output current cannot be delivered, the DC/DC converter resets the signal STB and a DC/DC interrupt is issued to the processor via IRQ SFR IRQ1.5. In this case, the microcontroller should switch off the different loads and switch to normal mode.

6.22.4.4 Off mode

Off mode can only be entered by setting the off bit in DCCON0 by software. The DC/DC converter waits for 15 periods of the 76.8 kHz clock before it sets V_{DD} to V_{BAT} and switches off completely (see Fig.41). In the off mode the PMOS is conducting and therefore it is guaranteed that V_{DD} never drops below $V_{BAT} - 100$ mV. When the DC/DC converter is in off mode, one of the following events can restart the converter:

- P1X (independent from interrupt enabling or polarity)
- Minute
- Wake-up
- RESETIN pulse.

6.22.5 VOLTAGE/CURRENT RIPPLE

The ripples are determined by V_{BAT}, inductance L, C_o, ESR (Equivalent Series Resistance of C_o, switching frequency and the load current I_L. The ripples are illustrated in Fig.43. If ESR = 0 Ω, then $V_{ripple} = \Delta V$.

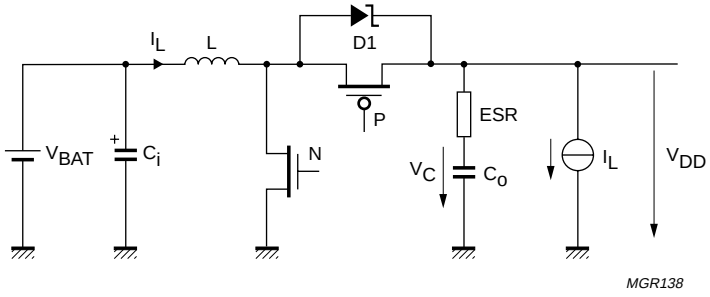


Fig.42 Circuit to analyse ripples.

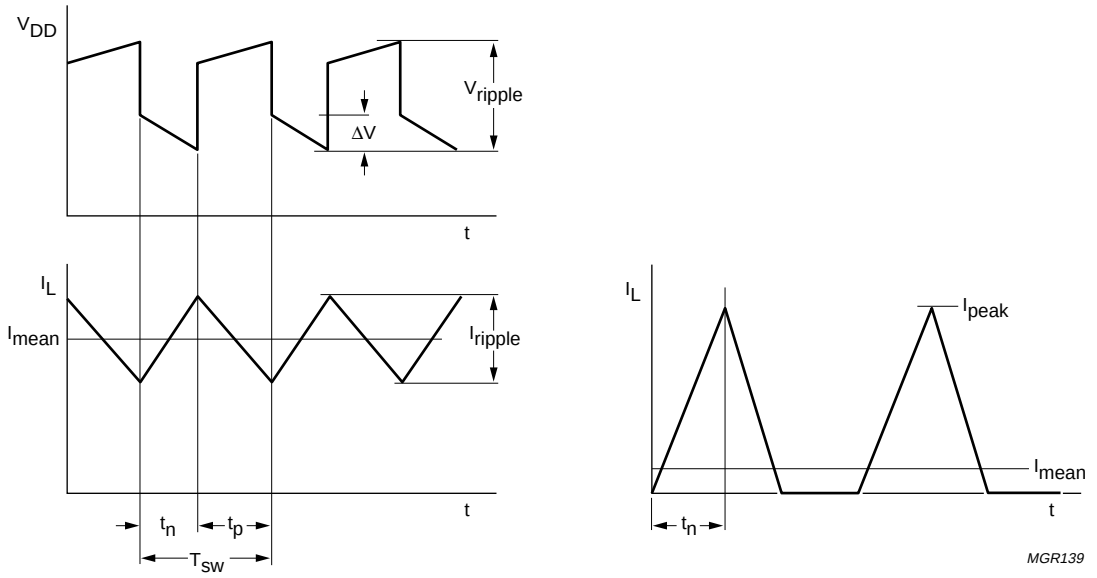


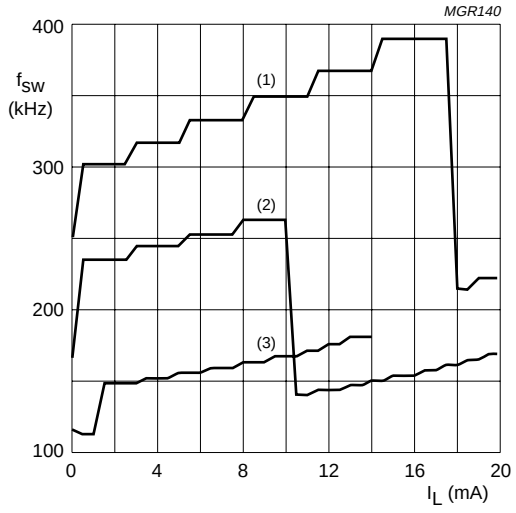
Fig.43 zoom in on the voltage and current ripples.

Table 54 Ripples in normal operation mode

MODE			
STANDBY		**NORM**	
$I_{peak} = V_{BAT} \times \frac{t_n}{L}$	t_n = 6.51 µs	$I_{ripple} = V_{BAT} \times \frac{t_n}{L}$	t_n = 1, 2 or 4 µs
		$I_{Lmean} = \frac{I_L}{D_p}$	$0.2 \leq D_p \leq 0.73$
$\Delta V = \frac{I_L \times t_n}{C_o}$	t_n = 6.51 µs	$\Delta V = \frac{I_L \times t_n}{C_o}$	t_n = 1, 2 or 4 µs
$V_{ripple} = \frac{V_{BAT} \times t_n}{L} \times ESR$	t_n = 6.51 µs	$V_{ripple} = \left(I_{mean} + \frac{1}{2} \times \frac{V_{BAT} \times t_n}{L} \right) \times ESR$	t_n = 1, 2 or 4 µs

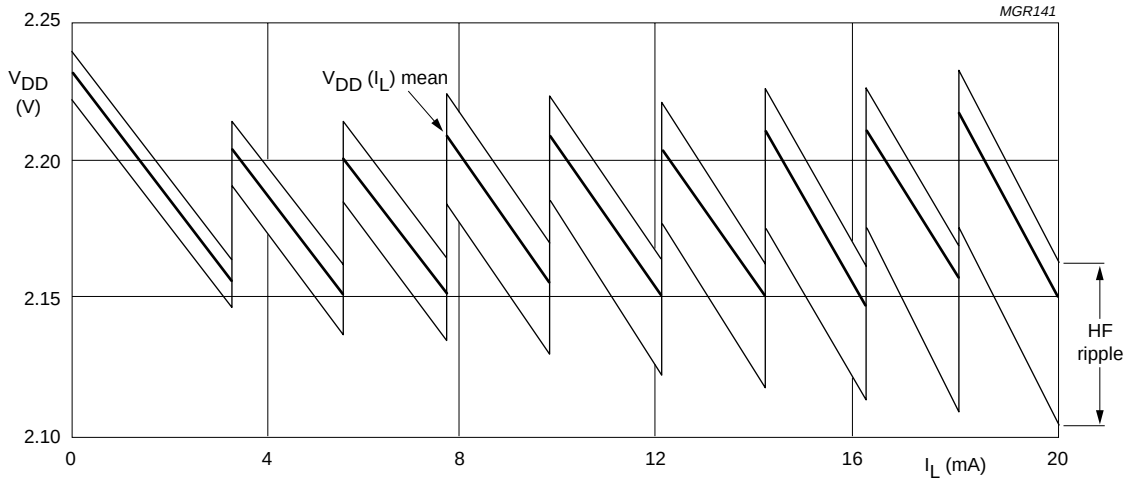
6.22.6 SWITCHING FREQUENCIES

Depending on the load and more importantly on the battery voltage the controller uses different on and off-times for the NMOS and PMOS transistors. This results in different switching frequencies. If the 6 MHz ring oscillator is trimmed to 6 MHz (see Section 6.12) the switching frequency is 120 kHz ≤ f_{sw} ≤ 400 kHz. A typical frequency behaviour is shown in Fig.44.



L = 470 µH, SRL = 5 Ω, C_o = 4.7 µF, ESR = 0.5 Ω.
(1) V_{BAT} = 1.5 V.
(2) V_{BAT} = 1.2 V.
(3) V_{BAT} = 1.0 V.

Fig.44 Switching frequencies.



V_{BAT} = 1.2 V; L = 470 µH; SRL = 5 Ω; C_o = 4.7 µF; ESR = 0.5 Ω.

Fig.45 V_{DD} as a function of load current.

6.22.7 V_{DD} ADJUSTMENT

V_{DD} can be shifted in four steps by adjusting the band gap voltage. The band gap voltage is set with the two bits VBG1 and VBG0 in DCCON1 according to Table 55.

Table 55 V_{DD} adjustment

VBG1	VBG0	OUTPUT VOLTAGE
0	0	V_{DD}
0	1	V_{DD} – 50 mV
1	0	V_{DD} + 50 mV
1	1	V_{DD} + 100 mV

6.22.8 BATTERY LOW MEASUREMENT

Battery low measurement is enabled by setting the SBLI bit in DCCON0. 0.5 ms after setting SBLI to logic 1 the BLI bit in DCCON0 contains the measurement result. When BLI = 0 the battery voltage is below 1.1 V. When BLI = 1 V_{BAT} is above 1.1 V. When SBLI = 1 V_{BAT} is measured continuously. Setting SBLI to logic 0 disables the V_{BAT} comparator and BLI is set to logic 1. After a reset pulse at RESETIN, SBLI is reset to logic 0.

6.22.9 DC/DC CONTROL REGISTER (DCCON0)

The DCCON0 special function register is used to control the operation of the on-chip DC/DC converter.

Table 56 DC/DC Control Register (DCCON0, SFR address D1H)

7	6	5	4	3	2	1	0
OFF	SBY	RXE	SBLI	–	–	STB	BLI

Table 57 Description of the DCCON0 bits

BIT	SYMBOL	FUNCTION
DCCON0.7	OFF	Writing this SFR bit to logic 1 puts the DC/DC converter in the off mode (independent of other control bits).
DCCON0.6	SBY	Writing this SFR bit to logic 1 puts the DC/DC converter in the standby mode, where the DC/DC converter is clocked from the 76.8 kHz oscillator and the ripple voltage will be higher. If the DC/DC converter is unable to deliver enough current in SBY mode, the software has to reset the SBY mode.
DCCON0.5	RXE	Writing this SFR bit to logic 1 uses the stored set of coefficients from a local register to force the DC/DC converter into the state which is appropriate for the required current. The contents of this local register are maintained when the DC/DC converter is set into off state. For the first time after connecting V_{BAT} a set of default coefficients is used. Writing this bit to logic 0 copies the actual coefficients used momentary by the DC/DC converter back to the local register.
DCCON0.4	SBLI	Writing this SFR bit to logic 1 enables the circuitry for measurement of the battery voltage. The new BLI value is valid 0.5 ms later. In order to make a new measurement, the receiver should draw current (continuous mode of DC/DC converter). If SBLI is logic 0 (BLI measurement disabled) BLI will go to HIGH.
DCCON0.3	–	Unused.
DCCON0.2	–	Unused.
DCCON0.1	STB	**Set by the DC/DC converter after power-up**. Reset by DC/DC converter if the converter is not able to deliver the required power. The signal is set in SBY and non SBY mode. This bit is read only.
DCCON0.0	BLI	**Battery low indicator**. Set by DC/DC converter if V_{BAT} < 1100 mV ±50 mV. This bit is read only.

6.22.10 DC/DC ADJUST CONTROL REGISTER (DCCON1)

The DCCON1 special function register is used to adjust the exact voltage levels of the on-chip DC/DC converter.

Table 58 DC/DC Adjust Control Register (DCCON1 and SFR address D2H)

7	6	5	4	3	2	1	0
VBG1	VBG0	VLO1	VLO0	–	–	–	–

Table 59 Description of the DCCON1 bits

BIT	SYMBOL	FUNCTION
DCCON1.7	VBG1	**Adjust for band gap voltage**; used to trim the band gap voltage [00] = 1.260 V, [01] = 1.233 V, [10] = 1.286 V, [11] = 1.312 V.
DCCON1.6	VBG0	
DCCON1.5	VLO1	**Adjust for DC/DC converter output voltage in standby mode**; [00] = 1.9 V, [01] = 2.0 V, [10] = 2.1 V, [11] = 2.2 V.
DCCON1.4	VLO0	
DCCON1.3	–	unused
DCCON1.2	–	unused
DCCON1.1	–	unused
DCCON1.0	–	unused

7 INSTRUCTION SET

The PBB family uses a powerful instruction set which permits the expansion of on-chip CPU peripherals and optimizes power consumption in Idle and active modes as well as byte efficiency and execution speed. Typical execution times and energy consumption at a V_{DD} of 2.2 V are given in Table 60. **Attention**: for most opcodes the numbers for execution speed and energy are also strongly dependant on the data (ADD, SUBB, DEC, INC, MUL, DIV, DA, conditional jumps etc.) and the operand address (CPU internal SFRs or SFRs in a peripheral block).

Table 60 Instruction set

MNEMONIC		DESCRIPTION	BYTES	EXEC. TIME [μs]	ENERGY [NJ]	OPCODE (HEX)
Arithmetic operations						
ADD	A,Rn	add register to A	1	0.498	1.831	2*
ADD	A,direct	add direct byte to A	2	0.631	2.501	25
ADD	A,@Ri	add indirect RAM to A	1	0.529	1.990	26, 27
ADD	A,#data	add immediate data to A	2	0.583	2.262	24
ADDC	A,Rn	add register to A with carry flag	1	0.508	1.864	3*
ADDC	A,direct	add direct byte to A with carry flag	2	0.637	2.525	35
ADDC	A,@Ri	add indirect RAM to A with carry flag	1	0.539	2.030	36, 37
ADDC	A,#data	add immediate data to A with carry flag	2	0.597	2.304	34
SUBB	A,Rn	subtract register from A with borrow	1	0.497	1.861	9*
SUBB	A,direct	subtract direct byte from A with borrow	2	0.630	2.527	95
SUBB	A,@Ri	subtract indirect RAM from A with borrow	1	0.528	2.021	96, 97
SUBB	A,#data	subtract immediate data from A with borrow	2	0.582	2.287	94
INC	A	increment A	1	0.459	2.475	04

MNEMONIC		DESCRIPTION	BYTES	EXEC. TIME [μs]	ENERGY [NJ]	OPCODE (HEX)
INC	Rn	increment register	1	0.457	1.737	0*
INC	direct	increment direct byte	2	0.586	1.982	05
INC	@Ri	increment indirect RAM	1	0.493	1.982	06, 07
DEC	A	decrement A	1	0.459	1.489	14
DEC	Rn	decrement register	1	0.457	1.74	1*
DEC	direct	decrement direct byte	2	0.590	2.488	15
DEC	@Ri	decrement indirect RAM	1	0.489	1.972	16, 17
INC	DPTR	increment data pointer	1	0.384	1.345	A3
MUL	AB	multiply A and B	1	0.378	1.242	A4
DIV	AB	divide A by B	1	0.733	2.532	84
DA	A	decimal adjust A	1	0.426	1.363	D4
Logic operations						
ANL	A,Rn	AND register to A	1	0.495	1.857	5*
ANL(1)	A,direct	AND direct byte to A	2	0.623	2.494	55
ANL	A,@Ri	AND indirect RAM to A	1	0.525	2.021	56, 57
ANL	A,#data	AND immediate data to A	2	0.583	2.272	54
ANL	direct,A	AND A to direct byte	2	0.650	2.639	52
ANL	direct,#data	AND immediate data to direct byte	3	0.719	3.138	53
ORL	A,Rn	OR register to A	1	0.459	1.605	4*
ORL(1)	A,direct	OR direct byte to A	2	0.584	2.248	45
ORL	A,@Ri	OR indirect RAM to A	1	0.486	1.767	46, 47
ORL	A,#data	OR immediate data to A	2	0.539	2.015	44
ORL	direct,A	OR A to direct byte	2	0.614	2.405	42
ORL	direct,#data	OR immediate data to direct byte	3	0.679	2.886	43
XRL	A,Rn	exclusive-OR register to A	1	0.459	1.715	6*
XRL(1)	A,direct	exclusive-OR direct byte to A	2	0.584	2.361	65
XRL	A,@Ri	exclusive-OR indirect RAM to A	1	0.486	1.873	66, 67
XRL	A,#data	exclusive-OR immediate data to A	2	0.540	2.128	64
XRL	direct,A	exclusive-OR A to direct byte	2	0.614	2.550	62
XRL	direct,#data	exclusive-OR immediate data to direct byte	3	0.679	3.017	63
CLR	A	clear A	1	0.374	1.265	E4
CPL	A	complement A	1	0.398	1.511	F4
RL	A	rotate A left	1	0.383	1.388	23
RLC	A	rotate A left through the carry flag	1	0.383	1.390	33
RR	A	rotate A right	1	0.382	1.381	03
RRC	A	rotate A right through the carry flag	1	0.383	1.382	13
SWAP	A	swap nibbles within A	1	0.371	1.394	C4

MNEMONIC		DESCRIPTION	BYTES	EXEC. TIME [μs]	ENERGY [NJ]	OPCODE (HEX)
Data transfer						
MOV	A,Rn	move register to A	1	0.377	1.406	E*
MOV	A,direct	move direct byte to A	2	0.509	2.080	E5
MOV	A,@Ri	move indirect RAM to A	1	0.408	1.568	E6, E7
MOV	A,#data	move immediate data to A	2	0.426	1.752	74
MOV	Rn,A	move A to register	1	0.344	1.347	F*
MOV	Rn,direct	move direct byte to register	2	0.602	2.654	A*
MOV	Rn,#data	move immediate data to register	2	0.415	1.839	7*
MOV	direct,A	move A to direct byte	2	0.477	2.024	F5
MOV	direct,Rn	move register to direct byte	2	0.536	2.294	8*
MOV	direct,direct	move direct byte to direct byte	3	0.661	2.950	85
MOV	direct,@Ri	move indirect RAM to direct byte	2	0.564	2.438	86, 87
MOV	direct,#data	move immediate data to direct byte	3	0.679	3.017	75
MOV	@RI,A	move A to indirect RAM	1	0.378	1.517	F6, F7
MOV	@Ri,direct	move direct byte to indirect RAM	2	0.633	2.629	A6, A7
MOV	@Ri,#data	move immediate data to indirect RAM	3	0.448	2.019	76, 77
MOV	DPTR,#data 16	load data pointer with a 16-bit constant	3	0.519	2.267	90
MOVC	A,@A+DPTR	move code byte relative to DPTR to A	1	0.775	3.570	93
MOVC	A,@A+PC	move code byte relative to PC to A	1	0.770	3.374	83
MOVX	A,@Ri	move external RAM (8-bit address) to A	1	0.707	2.732	E2, E3
MOVX	A,@DPTR	move external RAM (16-bit address) to A	1	0.710	2.605	E0
MOVX	@Ri,A	move A to external RAM (8-bit address)	1	0.629	2.595	F2, F3
MOVX	@DPTR,A	move A to external RAM (16-bit address)	1	0.631	2.439	F0
PUSH	direct	push direct byte onto stack	2	0.600	2.543	C0
POP	direct	pop direct byte from stack	2	0.606	2.548	D0
XCH	A,Rn	exchange register with A	1	0.513	1.847	C*
XCH	A,direct	exchange direct byte with A	2	0.645	2.526	C5
XCH	A,@Ri	exchange indirect RAM with A	1	0.544	2.024	C6, C7
XCHD	A,@Ri	exchange LOW-order nibble indirect RAM with A	1	0.486	1.904	D6, D7
Boolean variable manipulation						
CLR	C	clear carry flag	1	0.293	1.075	C3
CLR	bit	clear direct bit	2	0.597	2.509	C2
SETB	C	set carry flag	1	0.293	1.084	D3
SETB	bit	set direct bit	2	0.611	2.603	D2
CPL	C	complement carry flag	1	0.320	1.134	B3
CPL	bit	complement direct bit	2	0.583	2.471	B2
ANL	C,bit	AND direct bit to carry flag	2	0.540	2.187	82
ANL	C,/bit	AND complement of direct bit to carry flag	2	0.563	2.388	B0

MNEMONIC		DESCRIPTION	BYTES	EXEC. TIME [μs]	ENERGY [NJ]	OPCODE (HEX)
ORL[2]	C,bit	OR direct bit to carry flag	2	0.561	2.341	72
ORL	C,/bit	OR complement of direct bit to carry flag	2	0.561	2.341	A0
MOV	C,bit	move direct bit to carry flag	2	0.610	2.542	A2
MOV	bit,C	move carry flag to direct bit	2	0.610	2.542	92
Program and machine control						
ACALL	addr11	absolute subroutine call	2	0.840	3.384	•1 addr
LCALL	addr16	long subroutine call	3	1.082	4.562	12
RET		return from subroutine	1	1.082	4.562	22
RETI		return from interrupt	1	1.082	4.562	32
AJMP	addr11	absolute jump	2	0.670	2.524	♦1 addr
LJMP	addr16	long jump	3	0.840	3.384	02
SJMP	rel	short jump (relative address)	2	0.670	2.524	80
JMP	@A+DPTR	jump indirect relative to the DPTR	1	1.049	4.015	73
JZ	rel	jump if A is zero	2	0.639	2.224	60
JNZ	rel	jump if A is not zero	2	0.754	2.896	70
JC	rel	jump if carry flag is set	2	0.620	2.128	40
JNC	rel	jump if carry flag is not set	2	0.733	2.705	50
JB	bit,rel	jump if direct bit is set	3	0.788	3.095	20
JNB	bit,rel	jump if direct bit is not set	3	0.902	3.708	30
JBC	bit,rel	jump if direct bit is set and clear bit	3	0.894	3.520	10
CJNE	A,direct,rel	compare direct to A and jump if not equal	3	0.855	3.307	B5
CJNE	A,#data,rel	compare immediate to A and jump if not equal	3	0.794	3.024	B4
CJNE	Rn,#data,rel	compare immediate to register and jump if not equal	3	0.787	3.139	B*
CJNE	@Ri,#data,rel	compare immediate to indirect and jump if not equal	3	0.822	3.333	B6, B7
DJNZ	Rn,rel	decrement register and jump if not zero	2	0.857	3.474	D*
DJNZ	direct,rel	decrement direct and jump if not zero	3	0.991	4.178	D5
NOP		no operation	1	0.284	1.027	00

Notes

1. This opcode works in a slightly different way to a standard 80C51 CPU. If the direct field addresses one of the I/O ports (P0 to P3) then the standard 80C51 uses the port pin input state for the operation while the PCA5010 uses the SFR contents.
2. This opcode works in a slightly different way to a standard 80C51 CPU. If the direct bit field addresses one of the port bits, then the state of the corresponding port pin is written to the port SFR after execution of the instruction.

Table 61 Notation for data addressing modes

SYMBOL	DESCRIPTION
Rn	working registers R0 to R7
direct	128 internal RAM locations and any special function register (SFR).
@Ri	indirect internal RAM location addressed by register R0 or R1
#data	8-bit constant included in instruction
#data 16	16-bit constant included as bytes 2 and 3 of instruction
bit	direct addressed bit in internal RAM or SFR
addr16	16-bit destination address. Used by LCALL and LJMP. The branch will be anywhere within the 64 kbytes program memory address space.
addr11	11-bit destination address. Used by ACALL and AJMP. The branch will be within the same 2-kbyte page of program memory as the first byte of the following instruction.
rel	Signed (two's complement) 8-bit offset byte. Used by SJMP and all conditional jumps. Range is −128 to +127 bytes relative to first byte of the following instruction.

Table 62 Hexadecimal opcode cross-reference

SYMBOL	DESCRIPTION
*	8, 9, A, B, C, D, E and F
•	11, 31, 51, 71, 91, B1, D1 and F1
♦	01, 21, 41, 61, 81, A1, C1 and E1

7.1 Instruction Map

first hexadecimal character of opcode	second hexadecimal character of opcode															
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	AJMP addr11	LJMP addr16	RR A	INC A	INC direct	INC@Ri		INC Rn							
							0	1	0	1	2	3	4	5	6	7
1	JBC bit,rel	ACALL addr11	LCALL addr16	RRC A	DEC A	DEC direct	DEC@Ri		DEC Rn							
							0	1	0	1	2	3	4	5	6	7
2	JB bit,rel	AJMP addr11	RET	RL A	ADD A,#data	ADD A,direct	ADD A,@Ri		ADD A,Rn							
							0	1	0	1	2	3	4	5	6	7
3	JNB bit,rel	ACALL addr11	RETI	RLC A	ADDC A,#data	ADDC A,direct	ADDC A,@Ri		ADDC A,Rn							
							0	1	0	1	2	3	4	5	6	7
4	JC rel	AJMP addr11	ORL direct,A	ORL direct,#data	ORL A,#data	ORL A,direct	ORL A,@Ri		ORL A,Rn							
							0	1	0	1	2	3	4	5	6	7
5	JNC rel	ACALL addr11	ANL direct,A	ANL direct,#data	ANL A,#data	ANL A,direct	ANL A,@Ri		ANL A,Rn							
							0	1	0	1	2	3	4	5	6	7
6	JZ rel	AJMP addr11	XRL direct,A	XRL direct,#data	XRL A,#data	XRL A,direct	XRL A,@Ri		XRL A,Rn							
							0	1	0	1	2	3	4	5	6	7
7	JNZ rel	ACALL addr11	ORL C,bit	JMP @A+DPTR	MOV A,#data	MOV direct,#data	MOV @Ri,#data		MOV Rn,#data							
							0	1	0	1	2	3	4	5	6	7
8	SJMP rel	AJMP addr11	ANL C,bit	MOVC A,@A+PC	DIV AB	MOV direct,direct	MOV direct,@Ri		MOV direct,Rn							
							0	1	0	1	2	3	4	5	6	7
9	MOV DPTR,#data 16	ACALL addr11	MOV bit,C	MOVC A,@A+DPTR	SUBB A,#data	SUBB A,direct	SUBB A,@Ri		SUBB A, Rn							
							0	1	0	1	2	3	4	5	6	7
A	ORL C,/bit	AJMP addr11	MOV C,bit	INC DPTR	MUL AB		MOV @Ri,direct		MOV Rn,direct							
							0	1	0	1	2	3	4	5	6	7
B	ANL C,/bit	ACALL addr11	CPL bit	CPL C	CJNE A,#data,rel	CJNE A,direct,rel	CJNE @Ri,#data,rel		CJNE Rn,#data,rel							
							0	1	0	1	2	3	4	5	6	7
C	PUSH direct	AJMP addr11	CLR bit	CLR C	SWAP A	XCH A,direct	XCH A,@Ri		XCH A,Rn							
							0	1	0	1	2	3	4	5	6	7
D	POP direct	ACALL addr11	SETB bit	SETB C	DA A	DJNZ direct,rel	XCHD A,@Ri		DJNZ Rn,rel							
							0	1	0	1	2	3	4	5	6	7
E	MOVX A,@DPTR	AJMP addr11	MOVX A,@Ri		CLR A	MOV * A,direct	MOV A,@Ri		MOV A,Rn							
			0	1			0	1	0	1	2	3	4	5	6	7
F	MOVX @DPTR,A	ACALL addr11	MOVX @Ri,A		CPL A	MOV direct,A	MOV @Ri,A		MOV Rn,A							
			0	1			0	1	0	1	2	3	4	5	6	7

* MOV A, ACC is not a valid instruction.

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8 LIMITING VALUES

According to the Absolute Maximum Ratings System (IEC 134); note 1.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{BAT}	battery supply voltage	–0.5	+2.0	V
V_{DD}	supply voltage	–0.5	+5.0	V
V_I	input voltage (all inputs)	–0.3	V_{DD} + 0.3	V
$I_{I/O}$	maximum sink/source current for all input/output pins	–10	+10	mA
I_{BAT}, I_{IND}	maximum supply current for pins V_{BAT} and VIND	–	100	mA
I_{DD}	maximum supply current for any supply pin	–	50	mA
P_{tot}	total power dissipation	–	100	mW
$V_{ESD(HBM)}$	maximum ESD stress level applied to V_{PP} pin using human body model	–	2000	V
$V_{ESD(MM)}$	maximum ESD stress level applied to V_{PP} pin using machine model	–	200	V
T_{stg}	storage temperature	–55	+125	°C
T_{amb}	operating ambient temperature (for all devices)	–10	+55	°C

Note

1. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise specified.

9 EXTERNAL COMPONENTS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Discrete components					
L	inductor	330	470	1000	µH
C_o	output capacitor	–	4.7	10.0	µF
R_{FB}	feedback oscillator resistance	2.0	2.2	–	MΩ
R_{X1}	parasitic serial resistance of quartz	–	–	20	kΩ

10 DC CHARACTERISTICS

V_{SS} = 0 V; V_{DD} = 2.2 V; V_{BAT} = 1.2 V; T_{amb} = −10 to +55 °C; all voltages referenced to V_{SS} unless otherwise specified; DC/DC converter configured as indicated in note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Battery supply						
V_{BAT}	battery operating voltage	note 2	0.9	1.2	1.6	V
$I_{BAT(reset)}$	static reset supply current	V_{BAT} = 1.2 V; pin RESETIN at V_{BAT}; XTL1 at V_{SS}; P1.6, P1.7; I, Q, $\overline{EA}$, TCLK, V_{PP} at V_{SS} or V_{DD}; all outputs and I/Os open-circuit	–	0.5	5	µA
$I_{DD(reset)}$	static reset supply current	V_{DD} = 2.2 V; pin RESETIN at V_{BAT}; XTL1 at V_{SS}; P1.6, P1.7, I, Q, $\overline{EA}$, TCLK, V_{PP} at V_{SS} or V_{DD}; all outputs and I/Os open-circuit	–	0.5	10	µA
R_{NFET}	NFET pin-to-pin resistance	T_{amb} = 25 °C; V_{DD} = 2.2 V; note 3	–	1.1	2	Ω
R_{PFET}	PFET pin-to-pin resistance	T_{amb} = 25 °C; V_{DD} = 2.2 V; note 3	–	1.2	2	Ω
$I_{L(NFET)}$	NFET leakage current		–	–	1	µA
$I_{L(PFET)}$	PFET leakage current		–1	–	–	µA
$I_{NFET(max)}$	maximum allowed NFET current		–	–	50	mA
$I_{PFET(max)}$	maximum allowed PFET current		–	–	50	mA
DC/DC converter in off mode						
V_{DD}	DC supply voltage output		V_{BAT} − 0.1	–	V_{BAT}	V
$I_{BAT(off)}$	current consumed from V_{BAT} by the DC/DC converter itself	V_{DD} = V_{BAT}; all inputs at V_{SS} or V_{DD}; all outputs and I/Os open-circuit	–	6	–	µA
DC/DC converter in standby mode						
V_{DD}	DC supply voltage generated by the on-chip DC/DC converter for the PCA5010 and external chips	note 4; programmable in 4 steps	1.8	1.9	2.3	V
		1.9: [VLO, VLO] = 00	–	1.9	–	V
		2.0: [VLO, VLO] = 01	–	2.0	–	V
		2.1: [VLO, VLO] = 10	–	2.1	–	V
		2.2: [VLO, VLO] = 11	–	2.2	–	V
V_{DROP}	DC voltage drop due to load	I_L = 500 µA; notes 4 and 5	–	–	100	mV
$V_{ripple(p-p)}$	ripple voltage (peak-to-peak value)	notes 5 and 6	–	50	–	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{BAT(stb)}$	current consumed from V_{BAT} by the DC/DC converter itself	T_{amb} = 25 °C; notes 7 and 8	–	25	–	µA
$I_{DD(max)(stb)}$	maximum delivered continuous supply current	V_{BAT} = 0.9 V; R_s = 8 Ω; notes 8 and 9; see Fig.38	1	–	–	mA
$\eta_{(stb)}$	efficiency of DC/DC converter in standby mode	V_{BAT} = 1.2 V; I_{DD} = 100 µA; note 8	–	80	–	%
DC/DC converter in high current mode (non standby)						
V_{DD}	DC supply voltage generated by the on-chip DC/DC converter for the PCA5010 and external chips	note 4	2.2 – 6%	2.2	2.2 + 6%	V
$V_{DD(av)}$	mean DC voltage	notes 4 and 5	2.1	2.2	2.3	V
$V_{HFripple(p-p)}$	ripple voltage for frequencies above 20 kHz (peak-to-peak value)	notes 5 and 8	–	–	100	mV
$V_{LFripple(p-p)}$	low frequency ripple voltage caused by load variations (peak-to-peak value)	notes 3, 5 and 8	–	–	100	mV
$I_{BAT(norm)}$	current consumed from V_{BAT} by the DC/DC converter itself	T_{amb} = 25 °C; notes 8 and 10; see Fig.51	–	110	–	µA
$I_{DD(max)}$	maximum delivered supply current	V_{BAT} = 0.9 V; R_s= 8 Ω; notes 8 and 9; see Fig.37	10	–	–	mA
		V_{BAT} = 1.0 V; R_s = 5 Ω; notes 8 and 9	20	–	–	mA
$\eta_{(norm)}$	efficiency of DC/DC converter	note 8				
		$V_{BAT} \geq$ 1.2 V; I_{DD} = 3 mA	–	90	–	%
		$V_{BAT} \geq$ 1.2 V; I_{DD} = 10 mA	–	85	–	%
		V_{BAT} = 0.9 V; I_{DD} = 3 mA	–	85	–	%
		V_{BAT} = 0.9 V; I_{DD} = 10 mA	–	75	–	%
External supply current from V_{DD} = 2.2 V and V_{BAT} = 1.2 V						
V_{DD}	DC supply voltage (V_{DD} and V_{DDA} pins)	note 11; see Fig.64	2.2	2.2	2.5	V
I_{BAT}	operating battery current	T_{amb} = 25 °C; 76.8 kHz quartz	–	2	–	µA
$I_{DD(stb)}$	operating standby mode supply current from V_{DD}	T_{amb} = 25 °C; note 7	–	12	–	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{DD(RX)}$	operating receive mode supply current from V_{DD}	T_{amb} = 25 °C; note 10	–	85	–	µA
Supply current from internal or external V_{DD} = 2.2 V						
$I_{DD(micro)}$	I_{DD} due to operation of microcontroller	T_{amb} = 25 °C; note 12	–	0.7	–	mA/MIPS
$I_{DD(UART)}$	increase in I_{DD} due to operation of the UART	T_{amb} = 25 °C	–	5	–	µA
$I_{DD(IIC)}$	increase in I_{DD} due to operation of the I^2C-bus master	T_{amb} = 25 °C	–	20	–	µA
$I_{DD(T0)}$	increase in I_{DD} due to operation of timer/counter0	T_{amb} = 25 °C	–	0	–	µA
$I_{DD(T1)}$	increase in I_{DD} due to operation of timer/counter1	T_{amb} = 25 °C	–	2	–	µA
$I_{DD(AFC)}$	supply current due to operation of AFC-DAC	T_{amb} = 25 °C	–	60	–	µA
$I_{DD(SBLI)}$	supply current due to battery measurement active (SBLI = 1)	T_{amb} = 25 °C	–	20	–	µA
$I_{DD(6MHz)}$	increase in I_{DD} due to activation of 6 MHz oscillator in standby mode	T_{amb} = 25 °C; frequency adjusted to 6 MHz	–	50	–	µA
OTP programming (OTP data retention can only be guaranteed if the devices are preprogrammed by Philips Semiconductors; data retention cannot be guaranteed for customer programmed samples)						
$V_{DD(prog)}$	supply voltage during programming	note 11	2.2	–	3.6	V
V_{PP}	program supply voltage		12.5	–	13	V
I_{PP}	program supply current	note 13	–	24	–	mA
$T_{amb(prog)}$	operating ambient temperature during programming		21	–	27	°C
Band gap (reference voltage for all comparators)						
V_{BG}	band gap voltage	[VBG1, VBG0] = 00	1.23	1.26	1.29	V
		[VBG1, VBG0] = 01	–	1.233	–	V
		[VBG1, VBG0] = 10	–	1.286	–	V
		[VBG1, VBG0] = 11	–	1.312	–	V
Initial V_{DD} OK detection						
$V_{DD(OK)}$	V_{DD} OK indication	T_{amb} = 25 °C	1.5	1.85	2.0	V
Battery low indicator						
V_{BLI}	battery low indication	[VBG1, VBG0] = 00	1.05	1.1	1.15	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital input pins I(D1), Q(D0) and TCLK						
V_{IL}	LOW-level input voltage		–	–	$0.2V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.8V_{DD}$	–	–	V
I_L	leakage current	$V_I = V_{DD}$ or V_{SS}	–0.1	–	0.1	µA
Digital input pin RESETIN						
V_{IL}	input low level		–	–	$0.2V_{BAT}$	V
V_{IH}	input high level		$0.8V_{BAT}$	–	–	V
I_L	leakage current	$V_I = V_{DD}$ or V_{SS}	–0.1	–	0.1	µA
Digital input/output pin $\overline{EA}$						
V_{IL}	LOW-level input voltage	output not sinking current	–	–	$0.2V_{DD}$	V
V_{IH}	HIGH-level input voltage	output not sinking current	$0.8V_{DD}$	–	–	V
$I_{(o)sink}$	output sink current	V_{DD} = 2.2 V; V_I = 0.4 V	0.75	–	–	mA
$I_{(o)source}$	output source current	V_{DD} = 2.2 V; $V_I = V_{DD} - 0.4$ V	–	–	–0.75	mA
$I_{NMOS(h)}$	NMOS hold current	V_{DD} = 2.2 V; V_I = 0.6 V	–	–	200	µA
$I_{PMOS(h)}$	PMOS hold current	V_{DD} = 2.2 V; $V_I = V_{DD} - 0.6$ V	–200	–	–	µA
Digital output pin $\overline{RESOUT}$						
$I_{(o)sink}$	output sink current	V_{DD} = 2.2 V; V_I = 0.4 V	1.5	–	–	mA
$I_{(o)source}$	output source current	V_{DD} = 2.2 V; $V_I = V_{DD} - 0.4$ V	–	–	–1.5	mA
Digital input/output pins $\overline{PSEN}$						
V_{IL}	LOW-level input voltage	output not sinking current	–	–	$0.2V_{DD}$	V
V_{IH}	HIGH-level input voltage	output not sinking current	$0.8V_{DD}$	–	–	V
$I_{(o)sink}$	output sink current	V_{DD} = 2.2 V; V_I = 0.4 V	0.75	–	–	mA
$I_{(o)source}$	output source current	V_{DD} = 2.2 V; $V_I = V_{DD} - 0.4$ V	–	–	–0.75	mA
I_{pu}	weak pull-up current	V_{DD} = 2.2 V; V_I = 0 V	–20	–7	–2	µA
Digital input/output pins ALE						
V_{IL}	LOW-level input voltage	output not sinking current	–	–	$0.2V_{DD}$	V
V_{IH}	HIGH-level input voltage	output not sinking current	$0.8V_{DD}$	–	–	V
$I_{(o)sink}$	output sink current	V_{DD} = 2.2 V; V_I = 0.4 V	1.5	–	–	mA
$I_{(o)source}$	output source current	V_{DD} = 2.2 V; $V_I = V_{DD} - 0.4$ V	–	–	–1.5	mA
I_{pu}	weak pull-up current	V_{DD} = 2.2 V; V_I = 0 V	–20	–7	–2	µA
Microcontroller input/output ports P0, P1 and P2 pins (except P1.6 and P1.7)						
V_{IL}	LOW-level input voltage	output not sinking current	–	–	$0.2V_{DD}$	V
V_{IH}	HIGH-level input voltage	output not sinking current	$0.8V_{DD}$	–	–	V
$I_{(o)sink}$	output sink current	V_{DD} = 2.2 V; V_I = 0.4 V	0.75	–	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{(o)source}$	output source current	V_{DD} = 2.2 V; $V_I = V_{DD} - 0.4$ V	–	–	–0.75	mA
I_{pu}	weak pull-up current	V_{DD} = 2.2 V; V_I = 0 V	–20	–7	–2	µA
$I_{PMOS(h)}$	PMOS hold current	V_{DD} = 2.2 V; $V_I = V_{DD}/2$	–200	–70	–20	µA
Microcontroller output port P3 pins						
$I_{(o)sink}$	output sink current	V_{DD} = 2.2 V; V_I = 0.6 V	4	–	–	mA
$I_{(o)source}$	output source current	V_{DD} = 2.2 V; $V_I = V_{DD} - 0.6$ V	–	–	–6	mA
Open drain pins SDA and SCL (P1.6 and P1.7)						
V_{IL}	LOW-level input voltage	output not sinking current	–	–	$0.2V_{DD}$	V
V_{IH}	HIGH level input voltage	output not sinking current	$0.8V_{DD}$	–	–	V
I_L	leakage current	$V_I = V_{DD}$	–1	–	+1	µA
$I_{sink(stat)}$	static output sink current	V_{DD} = 2.2 V; V_I = 0.4 V	2.25	–	–	mA
$I_{sink(stat)(sc)}$	static output sink short-circuit current	V_{DD} = 2.2 V; $V_I = V_{DD}$	2.2	6	14	mA
AT output pin						
$I_{(o)sink}$	output sink current	V_{DD} = 2.2 V; V_I = 0.4 V	3	–	–	mA
$I_{(o)source}$	output source current	V_{DD} = 2.2 V; $V_I = V_{DD} - 0.4$ V	–	–	–3	mA
76.8 kHz oscillator						
$V_{IL(XTL1)}$	LOW-level input voltage XTL1		–	–	0.3	V
$V_{IH(XTL1)}$	HIGH-level input voltage XTL1		1	–	–	V
$I_{LI(XTL1)}$	leakage current at XTL1	$V_I = V_{BAT}$ or V_{SS}	–1	–	+1	µA
I_{bias}	bias current from XTL2 to V_{SS}	V_{BAT} = 1.6 V; XTL1 at V_{SS}	0.5	0.8	1.1	µA
I_{op}	operating current consumption	V_{BAT} = 1.6 V; R_{FB} = 2.2 MΩ	–	2	–	µA
g_m	transconductance	I_o = ±0.3 µA	5	20	60	µA/V
V_{WP}	DC working point		–	550	–	mV
AFC-DAC						
V_{AFC}	resolution		–	$1/64 V_{DD}$	–	V
ΔAFC	deviation for codes between 010000 and 100000 from straight line		–0.25LSB	–	+0.25LSB	
$R_{L(DAC)}$	allowed resistive load at DAC output		10	–	–	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$C_{L(DAC)}$	allowed capacitive load at DAC output		–	–	50	pF
$I_{source(DAC)}$	AFCOUT source current	V_{DD} = 2.2 V; V_{AFCOUT} = V_{DD} – 0.4 V; code = 111111	–	–895	–100	μA
$I_{sink(DAC)}$	AFCOUT sink current	V_{DD} = 2.2 V; V_{AFCOUT} = 0.4 V; code = 000000	10	25	–	μA

Notes

1. DC/DC converter configured with inductor of L = 470 μH, SRL = 5 Ω, input capacitance of C_i = 4.7 μF, ESR = 0.5 Ω, V_{DD} output capacitor C_o = 4.7 μF, ESR = 0.5 Ω, R_{BAT} < 1 Ω.
2. The required V_{BAT} for starting the circuit after connecting it to the battery is 1.1 V. But once in place, the battery can be used until it is discharged to 0.9 V.
3. This parameter is not tested during production; it is guaranteed by design.
4. This parameter is not tested during production; it is covered by other measurements.
5. The accuracy of the voltage is defined by maximum offset and ripple voltage. DC offset is defined by the accuracy of the internal band gap reference and the offset of comparators, whereas the ripple voltage is defined by the limits of the allowed voltage window of the regulated V_{DD}.
6. The ripple in standby mode is defined by V_{BAT}, L, t_n and ESR (see Table 54).
7. PCA5010 set to standby mode by software: 76.8 kHz oscillator running, DC/DC converter running in standby mode, all timer/counters disabled except RTC, microcontroller Idle, all outputs open-circuit, no I_{DD} delivered to external circuits.
8. This parameter depends on external components and is not tested during production; hence no guarantee.
9. R_s = total series resistance = R_{BAT} + SRL + $R_{DS(on)}$ + ESR.
10. PCA5010 set to receive mode by software: 76.8 kHz and 6 MHz oscillator running, DC/DC converter running in normal mode, wake-up counter, clock compensation, watchdog timer, T0 and T1 enabled, demodulator set to direct input data, AFC disabled, microcontroller Idle, all outputs open-circuit, no I_{DD} delivered to external circuits.
11. The minimum supply voltage is determined by the start-up sequence of the device. When the start-up sequence is completed, the supply voltage can be lowered to 1.8 V.
12. The microcontroller operates with approximately 1.9 million instructions per second at a V_{DD} = 2.2 V. The current consumption at this V_{DD} is 0.7 mA/MIPS (peripheral blocks as e.g. timers, DC/DC converter, I^2C-bus, UART, demodulator etc., are excluded). The current required from V_{DD} is then 1.35 mA (typ.). This scales to

    $$I_{BAT} = \frac{V_{DD}}{V_{BAT}} \times I_{DD} = 2.5\ \text{mA}$$ sunk from V_{BAT}.

13. In mass program mode the current can increase to 100 mA.

11 AC CHARACTERISTICS

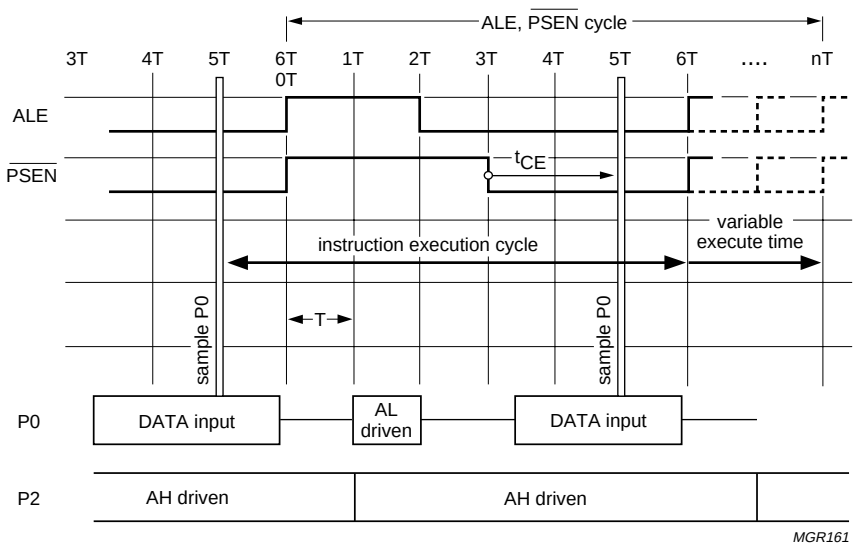
V_{BAT} = 0.9 to 1.6 V; V_{SS} = 0 V; T_{amb} = –10 to +55 °C; all voltages referenced to V_{SS} unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DC/DC converter; see note 1						
t_{on}	turn on time	off to normal operation; I_L < 500 µA; note 2	–	–	5	ms
$t_{ch(mode)}$	mode change time	enable to standby and reverse; note 2	–	–	1	ms
t_{step}	load step accommodation delay until stable	load step from 10 µA to 6 mA; note 3	–	–	1	ms
f_{sw}	switching frequency	in normal mode; note 2	120	250	400	kHz
t_{sw}	switching period	in standby mode; note 4	1 or 1.5 t_{XTL1}	–	–	µs
$t_{ch(L)}$	inductor charge time	in standby mode; note 4	–	0.5 or 1 t_{XTL1}	–	µs
RESET signal						
$t_{RESETIN(min)}$	minimum duration of RESETIN pulse		20	–	–	µs
Microcontroller						
$t_{instr(int)}$	internal instruction execution time	internal access, V_{DD} = 2.2 V; T_{amb} = 25 °C; note 5	–	550	–	ns
$t_{instr(ext)}$	external instruction execution time	external access, V_{DD} = 2.2 V; T_{amb} = 25 °C; note 5	–	650	–	ns
76.8 kHz oscillator						
f_{xtal}	crystal frequency	note 3	76784	76800	76816	Hz
$f_{i(max)}$	maximum input frequency through input buffer		–	–	100	kHz
C_1	input capacitance		–	10 ± 15%	–	pF
C_2	output capacitance		–	10 ± 15%	–	pF
6 MHz oscillator						
$f_{i(osc)}$	oscillator input frequency	[$\overline{SF4}$, SF3, SF2, SF1, SF0] = 00000 (reset condition)	3	5.4	8	MHz
		[$\overline{SF4}$, SF3, SF2, SF1, SF0] = 10000	1	2.7	5	MHz
		[$\overline{SF4}$, SF3, SF2, SF1, SF0] = 01111	6	7.6	11	MHz
$f_{i(osc)} \pm \Delta f$	adjusted frequency		5.85	6	6.15	MHz
$t_{d(en)}$	enable oscillator delay	note 2	–	20	30	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ZIF (I and Q) demodulator						
f_{offset}	offset from 0 frequency	note 2	6	–	–	kHz
$t_{(ENA-AVG)}$	ENA to valid AVG value	3 kHz offset; note 2	–	–	100	ms
t_{ENB}	ENB to valid demodulator output	note 2	–	–	1	symbol duration
t_{ENC}	ENB to correct recovered clock	note 2	phase error curves apply (see Fig.27)			
All outputs						
$t_{r,f}$	rise and fall times for outputs	C_L = 20 pF	–	15	–	ns
Open-drain pins SDA and SCL (P1.7 and P1.6)						
t_n	noise suppression filter		–	60	–	ns
$\Delta V/\Delta t$	slope for the falling edge	R_L = 20 kΩ; C_L = 50 pF; V_{DD} = 2.2 V	–	50	–	ns/V
dI/dt	slope for both edges	R_L = 20 kΩ; C_L = 50 pF	–	250	–	µA/ns
$I_{o(sink)(swL)}$	dynamic output sink current during switching low (Miller compensated)	V_{DD} = 2.2 V; R_L = 20 kΩ; C_L = 50 pF	–	2	–	mA
OTP programming characteristics						
$V_{SU;PP}$	V_{PP} set-up time		10	–	–	µs
$t_{W(prog)}$	program pulse width		100	–	–	µs
$t_{W(prog)(sec)}$	program pulse security bits		200	–	–	µs
$t_{W(prog)(rec)}$	program pulse recover time		1	–	–	µs
AFC-DAC						
$t_{start(DAC)}$	start-up time disabled DAC to stable output for code 111111	note 2	–	50	100	µs
PSRR	power supply ripple rejection (V_{DD} -> DAC)		–	0	–	dB
t_{slew}	slew time for analog output from 10 to 90% for a voltage step of 1 V	code 010000 <-> 110000	–	2.5	–	µs

Notes

1. DC/DC converter configured with inductor of L = 470 µH, SRL = 5 Ω, input capacitance of C_i = 4.7 µF, ESR = 0.5 Ω, V_{DD} output capacitor C_o = 4.7 µF, ESR = 0.5 Ω, R_{BAT} < 1 Ω.
2. This parameter is not tested during production; it is guaranteed by design.
3. This parameter depends on external components.
4. At high load or low battery voltage the inductor charge time can be extended to a full XTL1 period, while the minimum inductor discharge time is a half XTL1 period.
5. The execution time is strongly dependant on command type and addressing mode (see also Table 60).



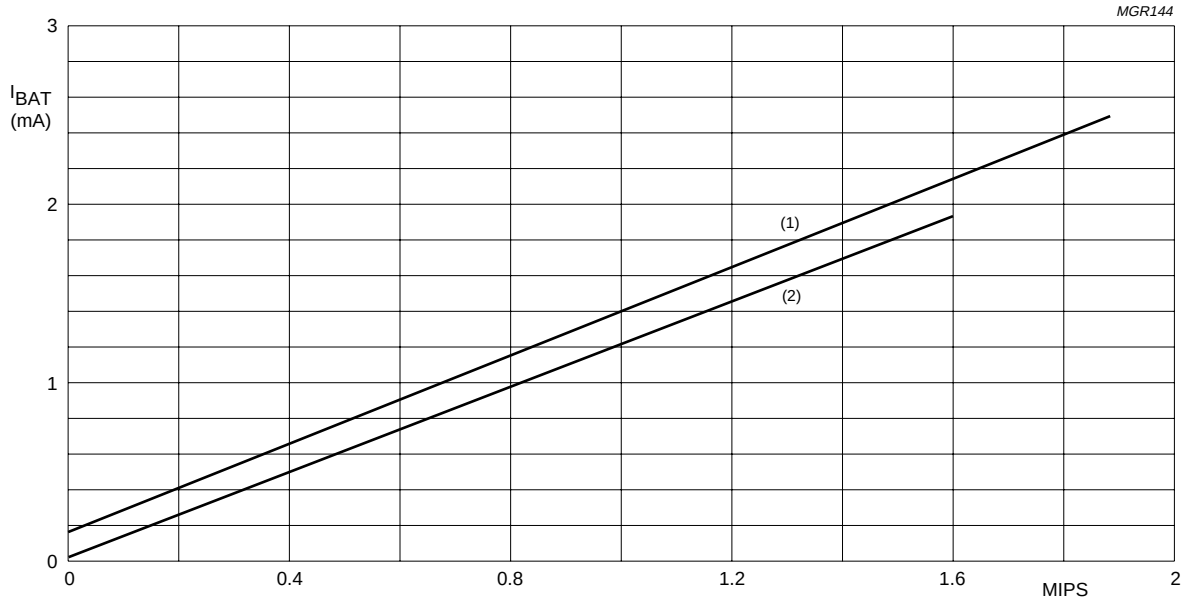
T being the half period of the internal 6 MHz oscillator for normal external access and of TCLK for emulation, programming and test modes.

The minimum duration of one cycle is 6T. It can be extended by increments of [0 to n]T if the execution of an instruction needs more time (dependant of V_{DD}, T, Temperature, Opcode).

Execution of an op-code goes in parallel with the external access cycle for the next sequential byte. Eventually an already fetched byte is discarded depending on the executed instruction (e.g. any jump or return).

Fig.46 External access timing.

12 CHARACTERISTIC CURVES

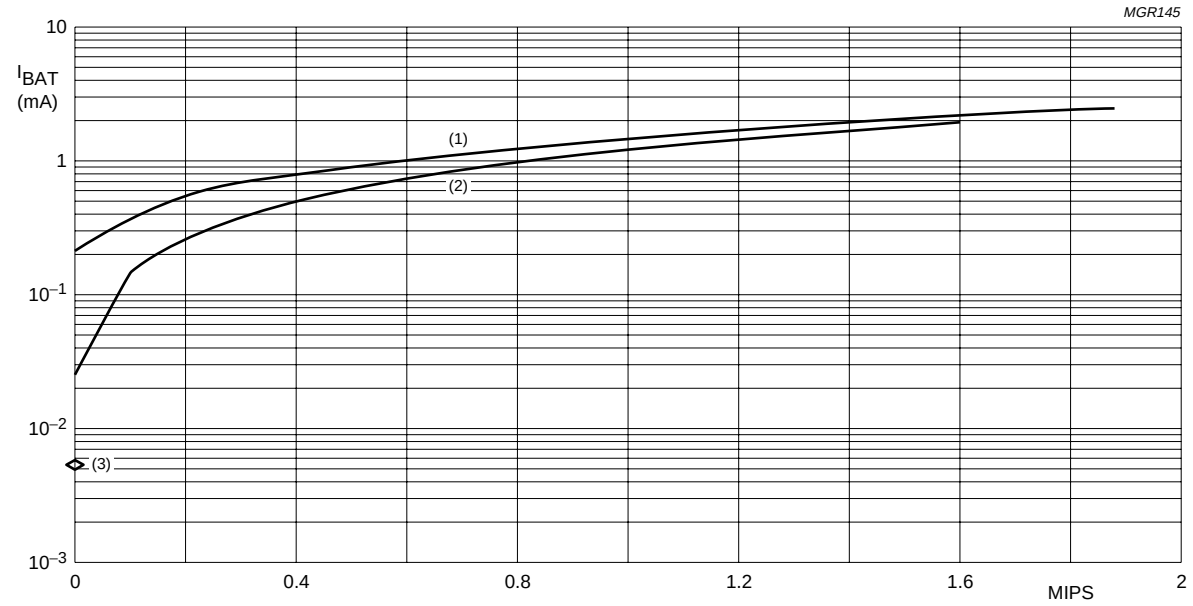


V_{BAT} = 1.2 V.

(1) DC/DC converter in normal mode.

(2) DC/DC converter in standby mode.

Fig.47 Measured battery current consumption as function of mean microcontroller instruction rate.



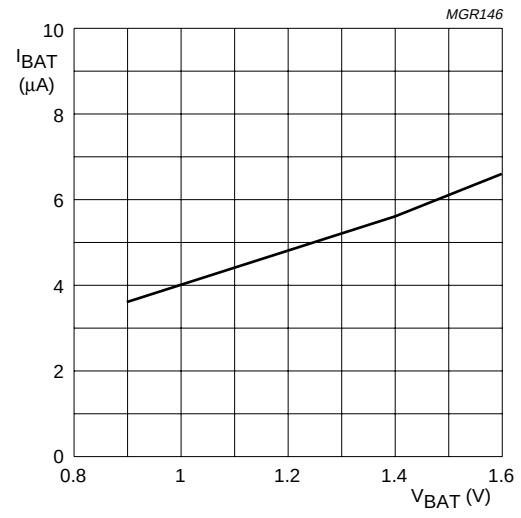
V_{BAT} = 1.2 V.

(1) DC/DC converter in normal mode.

(2) DC/DC converter in standby mode.

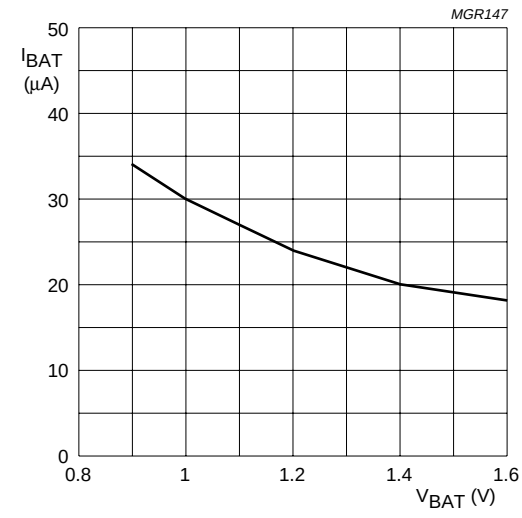
(3) DC/DC converter in off mode.

Fig.48 Measured battery current consumption as function of mean microcontroller instruction rate.



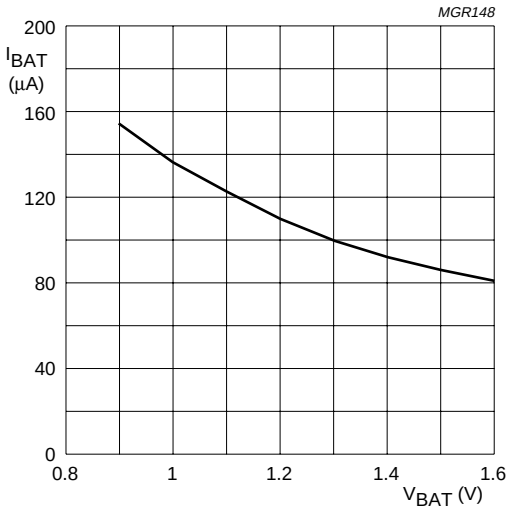
V_{DD} = V_{BAT}, microcontroller idle, all functions disabled.

Fig.49 Supply current in off mode.



V_{DD} = 1.9 V, microcontroller idle, all functions disabled.

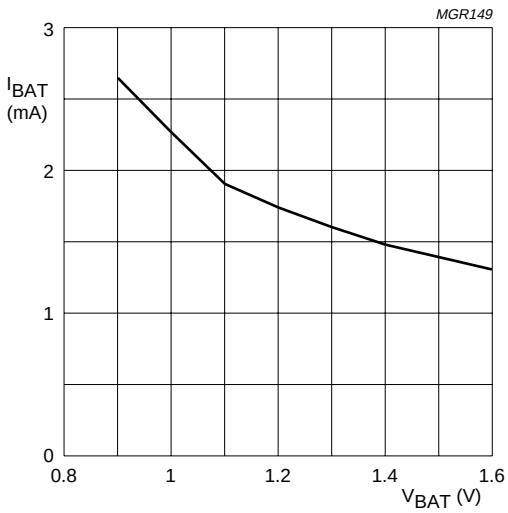
Fig.50 Supply current in standby mode.



V_{DD} = 2.2 V, microcontroller idle, all functions disabled.

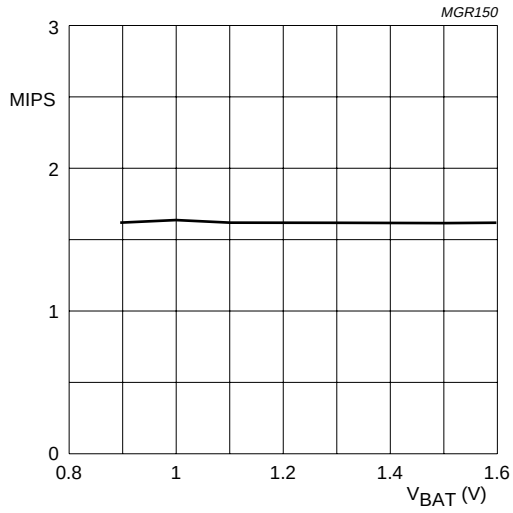
Note: This curve cannot be directly measured by varying V_{BAT}, because the shown current is the battery current in discontinuous mode. Changing the battery voltage can force the DC/DC converter to enter continuous mode.
At a given battery voltage a mode change from continuous to discontinuous mode happens only after a load reduction.

Fig.51 Supply current in normal mode.



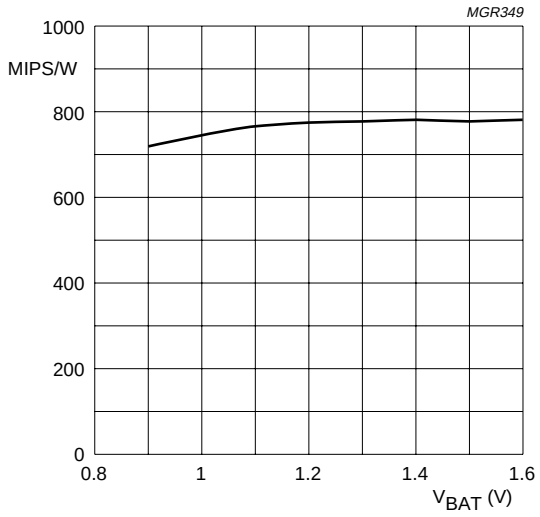
V_{DD} = 1.9 V, microcontroller running at approximately 1.6 MIPS, all other functions disabled.

Fig.52 Supply current in standby mode.



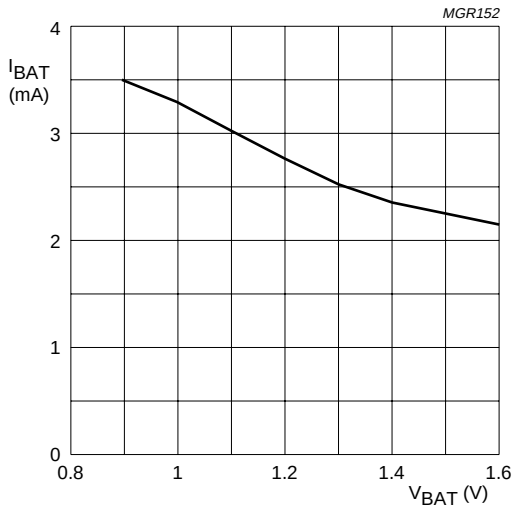
V_{DD} = 1.9 V, microcontroller running at maximum speed.

Fig.53 CPU speed performance with DC/DC in standby mode.



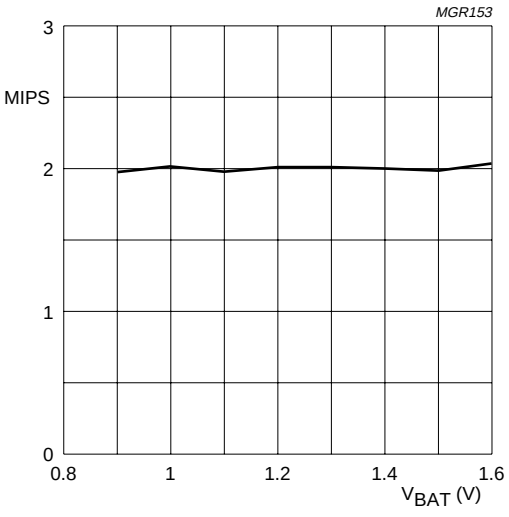
V_{DD} = 1.9 V, microcontroller running at maximum speed.

Fig.54 Overall power/speed performance with DC/DC in standby mode.



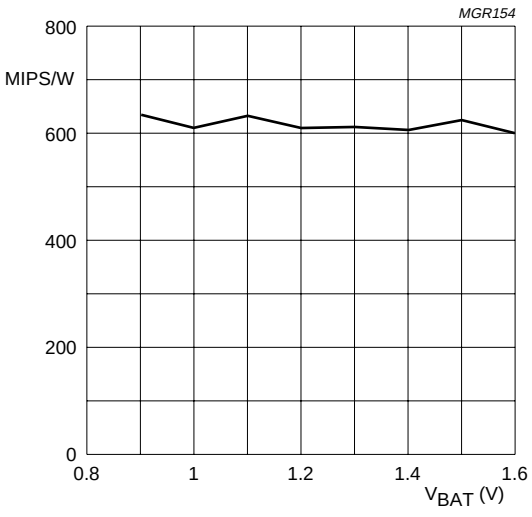
V_{DD} = 2.2 V, microcontroller running at approximately 2 MIPS, all other functions disabled.

Fig.55 Supply current in normal mode.



V_{DD} = 2.2 V, microcontroller running at maximum speed.

Fig.56 CPU speed performance with DC/DC converter in normal mode.



V_{DD} = 2.2 V, microcontroller running at maximum speed.

Fig.57 Overall power/speed performance with DC/DC converter in normal mode.

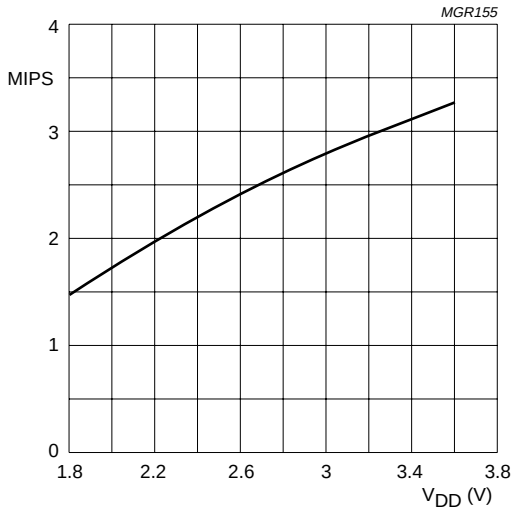


Fig.58 Speed performance PCA5010 when V_{DD} is externally supplied (DC/DC converter not used).

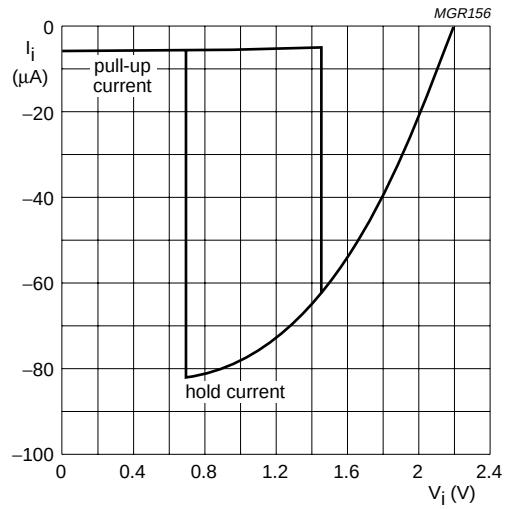


Fig.59 Typical impedance characteristic of standard port in input mode.

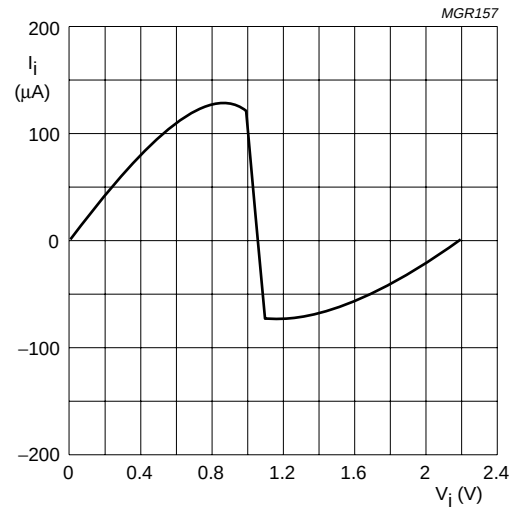
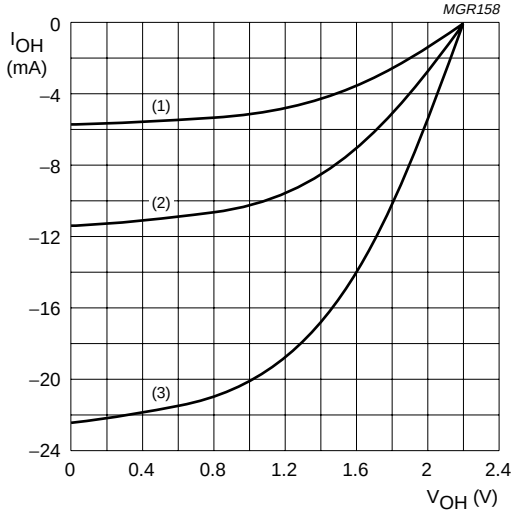
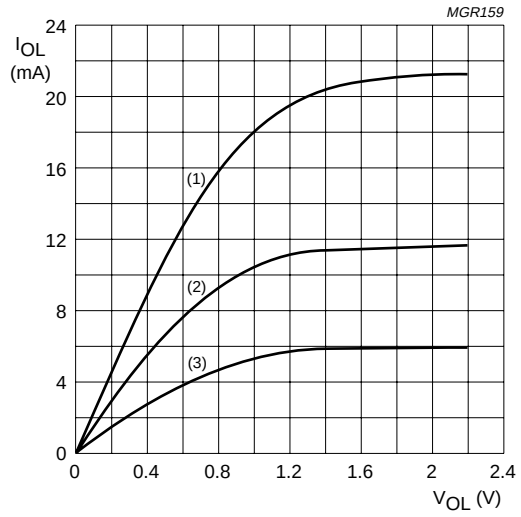


Fig.60 Typical impedance characteristic of $\overline{EA}$ pin in input mode.



(1) Pins P0.X, P1.X, P2.X, $\overline{PSEN}$ and $\overline{EA}$.
(2) Pins $\overline{RESOUT}$ and ALE.
(3) Pins P3.X and AT.

Fig.61 Typical output characteristics driven HIGH (digital output/port pins except P1.6 and P1.7).



(1) Pins P3.X and AT.
(2) Pins $\overline{\text{RESOUT}}$ and ALE.
(3) Pins P0.X, P1.X, P2.X, $\overline{\text{PSEN}}$ and $\overline{\text{EA}}$.

Fig.62 Typical output characteristics LOW (digital output/port pins except P1.6 and P1.7).

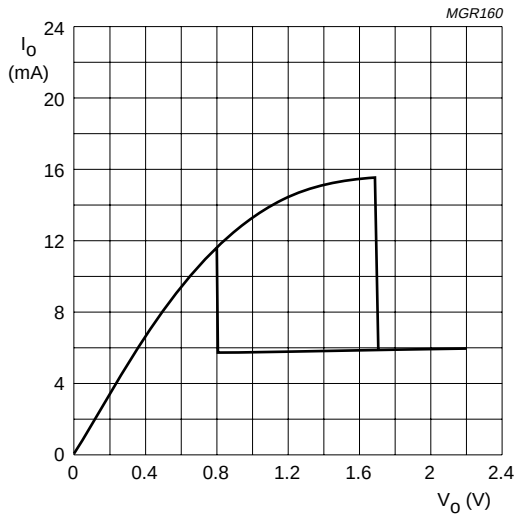


Fig.63 Typical output characteristics LOW for P1.6 and P1.7.

13 TEST AND APPLICATION INFORMATION

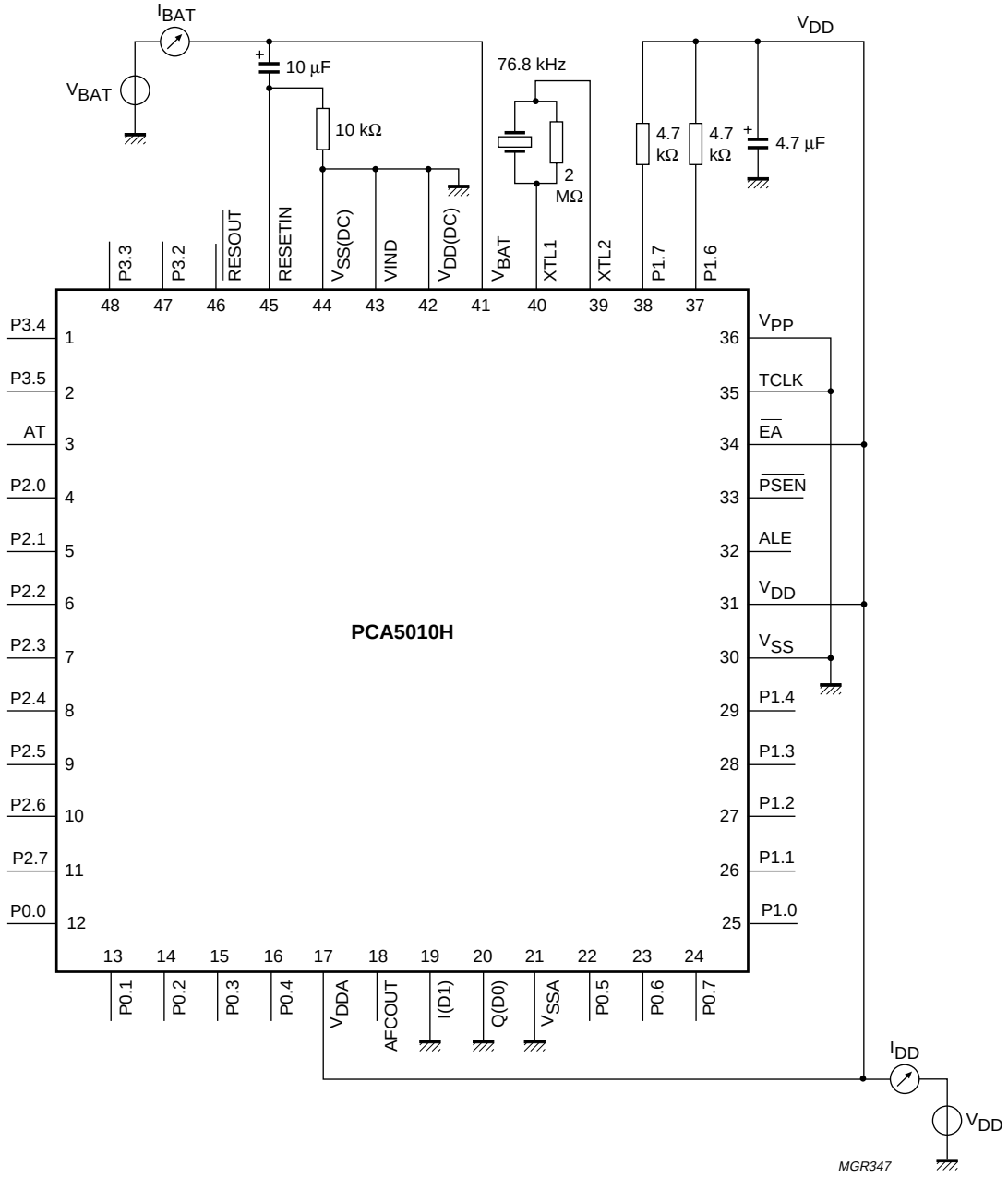


Fig.64 Test circuit for current measurements with external V_{DD} supply.

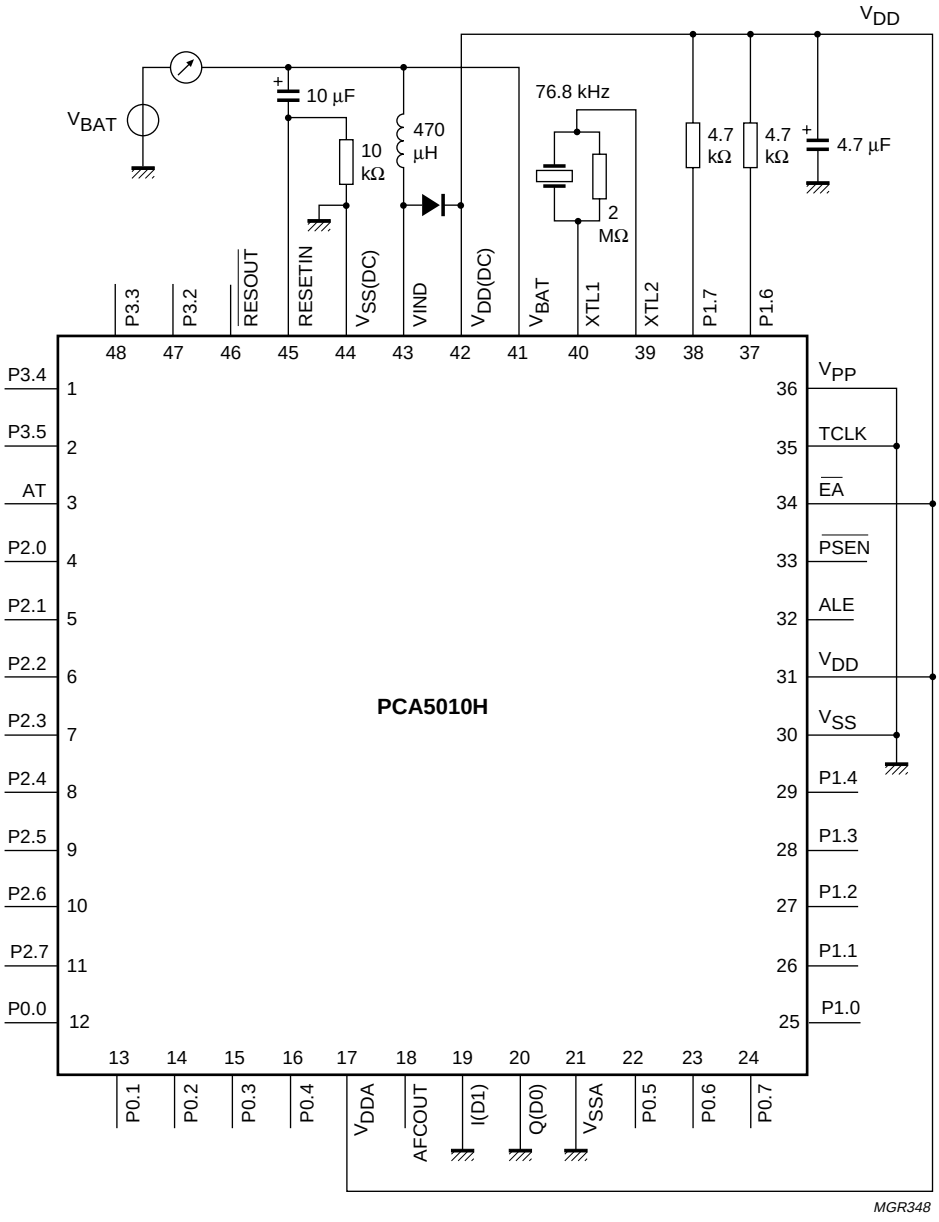


Fig.65 Test circuit for current measurements with on-chip DC/DC converter active.

14 APPENDIX 1: SPECIAL MODES OF THE PCA5010

14.1 Overview

During the rising edge of the external $\overline{\text{RESOUT}}$ signal, the state of the pins ALE, $\overline{\text{PSEN}}$, $\overline{\text{EA}}$ and P2.X is sampled and stored. The following decoding (ALE, $\overline{\text{PSEN}}$ and P2) is used to force the PCA5010 into different operating modes:

[1, 1, X] $\rightarrow$ RUN mode

[0, 1, X] $\rightarrow$ EMUlation modes (for P2 decoding refer to Metalink documents)

[1, 0, Y] $\rightarrow$ test mode, submode Y

[0, 0, X] $\rightarrow$ OTP parallel programming mode.

The customer will usually only see the normal RUN mode.

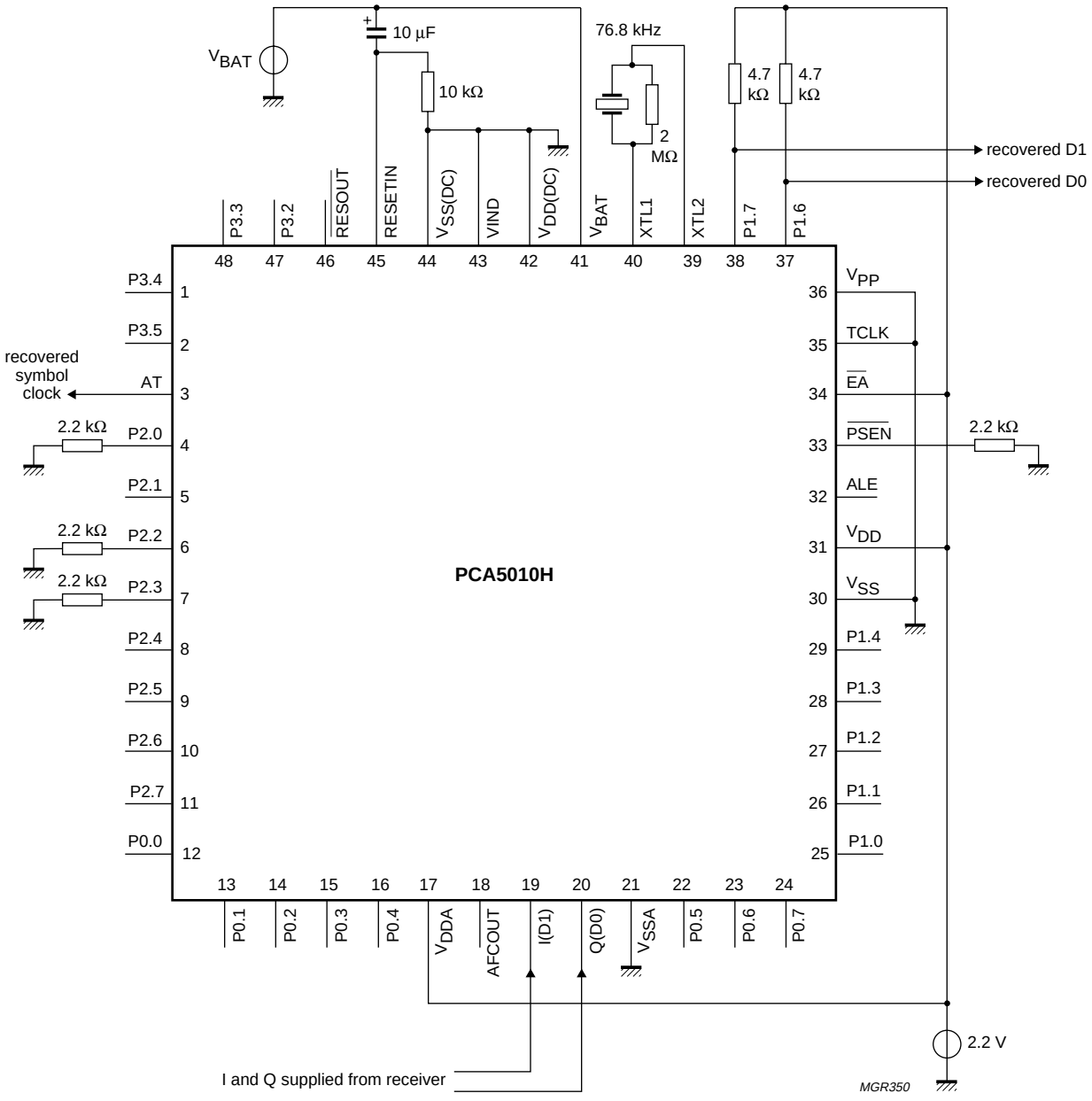
14.2 OTP parallel programming mode

The OTP parallel programming mode is used to access the on-chip OTP directly from the device pins for programming and verification. The OTP parallel programming mode and its initialization are explained in detail in Chapter 15.

14.3 Test modes

The test modes of the PCA5010 are used during the production test of the circuit. Test modes are not intended to be used by customers except test mode 2, the demodulator and clock recovery test mode.

Test mode 2 may be used by customers for BER measurements in closed-loop systems. The following application diagram (see Fig.66) shows an application which enters this mode during start-up. After the test mode is entered the PCA5010 starts execution of code from the internal program memory. This code must enable the demodulator and clock recovery in the required modes. If the microcontroller is requested to make port I/O, then a frequency of approximately 6 MHz with V_{DD} level needs to be supplied at the TCLK pin.



The OTP must contain code that enables the demodulator and clock recovery in the desired operating modes.

Fig.66 Application diagram for entering the demodulator test mode after reset.

15 APPENDIX 2: THE PARALLEL PROGRAMMING MODE

15.1 Introduction

This document describes the parallel programming mode of the PCA5010. Parallel programming mode is the mode where the OTP is programmed by an EPROM programmer or by a tester.

15.2 General description

The PCA5010 is packaged in a LQFP48 package. Port 0 and Port 2 are available for programming. To program the OTP of the PCA5010, multiplexing of addresses and data is necessary. Port 0 is a bidirectional data port, used for the memory addresses and the program and verify data. Port 2 is an input port which controls the parallel programming mode. A coarse block diagram of the OTP interface in parallel programming mode is given in Fig.67.

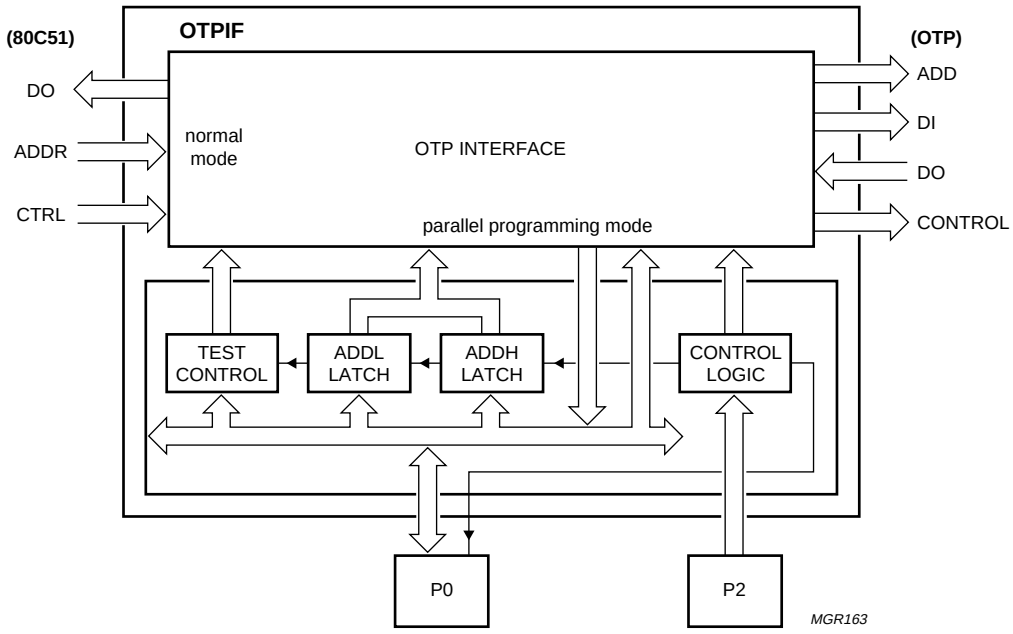


Fig.67 The OTP interface in parallel programming mode.

15.2.1 SIGNALS FOR THE PARALLEL PROGRAMMING MODE

In this configuration, the following signals are necessary to program the OTP:

Table 63 Pins for programming mode

OTP PIN	TYPE	EPROM PIN	DESCRIPTION	COMMENTS
V_{PP}	supply	V_{PP}	programming voltage	special pin/logic signal not time critical
V_{DD}	supply	V_{DD}	positive supply	
GND	supply	GND	negative supply	
P0.7 to P0.0	IO	A<14:0>	address	32 kbytes addresses available
		Q<7:0>	data-output	
		I<7:0>	data-input	
		PS<2:0>	security bits input	connected to P0.2 to P0.0 pins
		QS<2:0>	security bits output	
P2.0/LS0	input	–	latch select 0	latch select signals, see Table 64
P2.1/LS1	input	–	latch select 1	
P2.2/PGM	input	–	programming mode	
P2.3/RdStrb	input	CEP/MBPC	read/strobe	read enable clock (CEP) when PGM = 0; strobe for the latches when PGM = 1
P2.4/GBMbpB	input	GB	output enable not/ Mult.BProg Not	read EPROM and set P0 as output; multiple byte programming when PGM = 1
P2.5/WEB	input	WEB	write enable not	programs data if V_{PP} is present
P2.6/SEC	input	SEC	select security bits	see Section 15.10
P2.7/SIG	input	SIG	read signature bytes	see Section 15.9

The control signals GBMbpB, PGM, LS1 and LS0 can be used to select the latches of the interface block and the internal data latches of the OTP. Table 64 shows how the latches are selected.

RdStrb is used to open the selected latch. If PGM is not active the RdSTrb signal is used to start the OTP read cycle.

Table 64 Latch selection

P2.4/GBMbpB	P2.2/PGM	P2.1/LS1	P2.1/LS0	DESCRIPTION
X	0	X	X	no latches selected
1	1	0	0	select test control latch
X	1	0	1	select lower address latch
X	1	1	0	select upper address latch
0	1	1	1	select internal data latch in multi byte programming mode

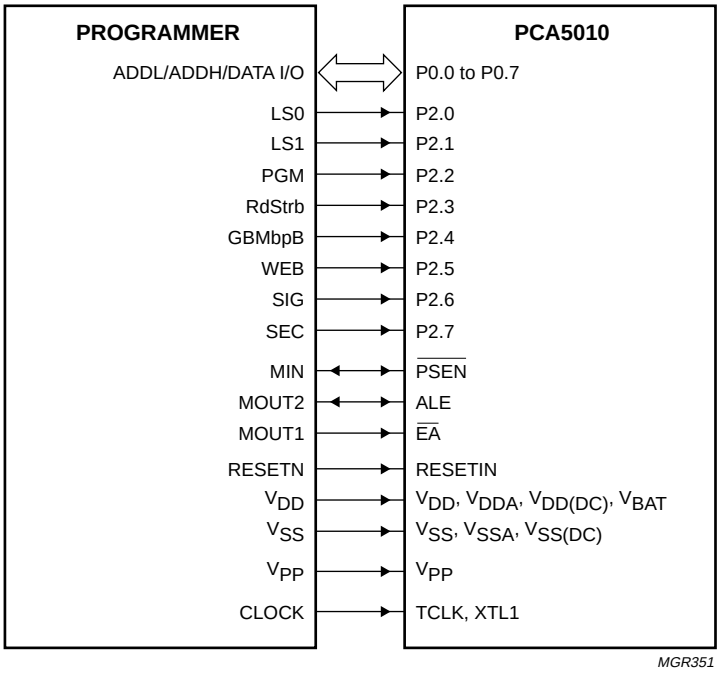


Fig.68 Parallel programming mode.

15.3 Entering the parallel programming mode

The parallel programming mode has been implemented as a general test mode of the PCA5010. This mode can be entered by applying 000 to pins $\overline{PSEN}$, ALE, and $\overline{EA}$ during reset. For the initializing sequence a clock of 76.8 kHz at XTL1 is expected and the supply voltage V_{DD} must be higher then 2.2 V. At the rising edge of $\overline{RESOUT}$ these signals are latched and the code 000 leads to parallel programming mode. The high voltage pin V_{PP} can be either HIGH or V_{DD}.

Since $\overline{PSEN}$ and ALE are output signals of the PCA5010 after reset, a pull-down (strong enough to overdrive the internal 100 µA pull-up of the PCA5010) should be used to drive the outputs LOW. Alternatively the LOW can be driven with a 3-state buffer which is enabled with $\overline{RESOUT}$ = LOW.

The microcontroller fetches instructions from Port 0 in external mode. Data fetching is controlled by $\overline{PSEN}$ and ALE. This is the standard data fetch in external mode. A clock has to be supplied to TCLK while entering the parallel programming mode. Before entering the parallel programming mode, Port 2 should be set to 30H and the microcontroller should be put in Idle mode by setting the bit PCON.0 (address 87H).

The test mode is activated by making $\overline{EA}$ equal to logic 1. The mode entering sequence is given in Table 65.

Before entering the parallel program mode Port 2 can be an output port (dependent on the reset configuration of this port). As soon as the parallel programmed mode is entered Port 2 is an input.

After entering the parallel programming mode this mode has to be initialized. The OTP test latch has to be loaded with code 01H to set the sense amplifiers in verify mode. Before a byte can be programmed a verify has to be performed to check if programming is not blocked by the security (see Section 15.10). The address of this verify cycle is not important and the address latches do not have to be loaded. After this initialization the PCA5010 is ready for programming. Parallel program initialization is shown in Fig.71.

The security check can be replaced by another read action e.g reading the security or signature bytes (see Section 15.9).

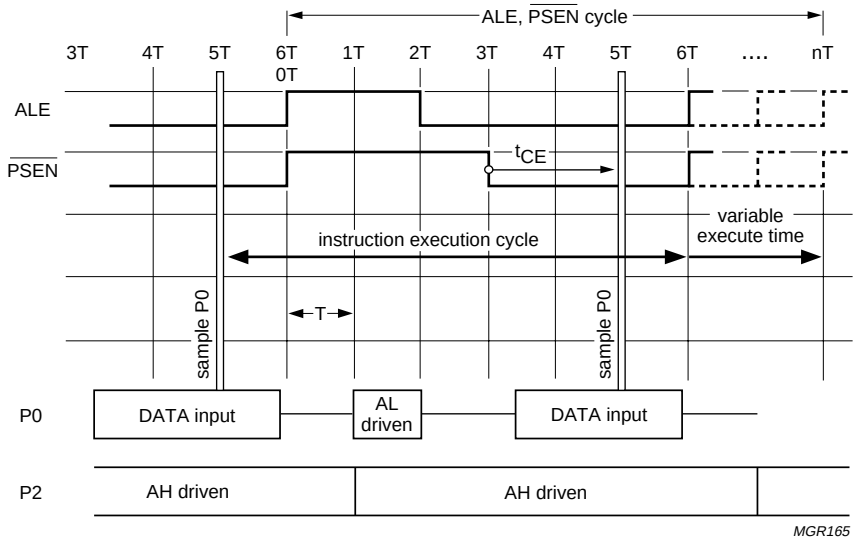
It should be noted that this paragraph is only applicable for the first series. It can be neglected in the future. To prevent problems with the self timed loop it is advised to set the circuit in DC read mode during verify. This is achieved by writing 09H instead of 01H into the OTP test latch.

Table 65 Entering the parallel programming mode; note 1

PINS $\overline{PSEN}$, ALE AND $\overline{EA}$	RESETIN	$\overline{RESOUT}$	PORT 0	DESCRIPTION
000	1	0	xx	reset
000	0	0	xx	259 or more slow clocks at XTL1
000	0	0 → 1	xx	prepare parallel programming mode, enter external access mode, now clocks must be provided on TCLK
zz0	0	1	02	LJMP 3000H
zz0	0	1	30	force P2 to 30H
zz0	0	1	00	
zz0	0	1	00	discard fetch cycle
zz0	0	1	75	MOV PCON, 01H
zz0	0	1	87	make microcontroller idle
zz0	0	1	01	
zz0	0	1	01	discard fetch cycle
zz1	0	1	xx	parallel programming mode active

Note

1. z = pin is output.



T being the half period of the clock signal supplied to TCLK.

The minimum duration of one cycle is 6T. It can be extended by increments of [0 to n]T if the execution of an instruction needs more time (dependant of V_{DD}, T, Temperature, Opcode).

Execution of an op-code goes in parallel with the external access cycle for the next sequential byte. Eventually an already fetched byte is discarded depending on the executed instruction (e.g. any jump or return).

Fig.69 External access timing for programming mode entry.

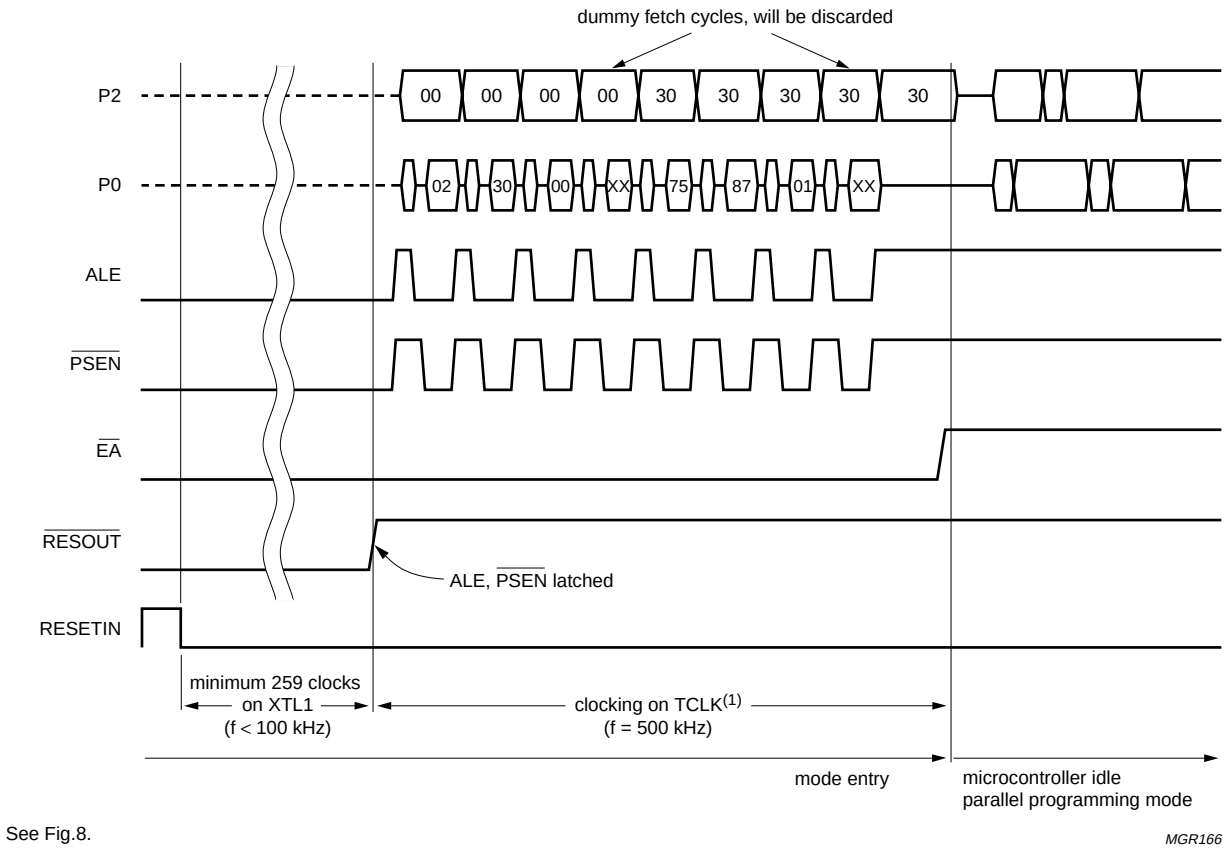


Fig.70 Program mode entry.

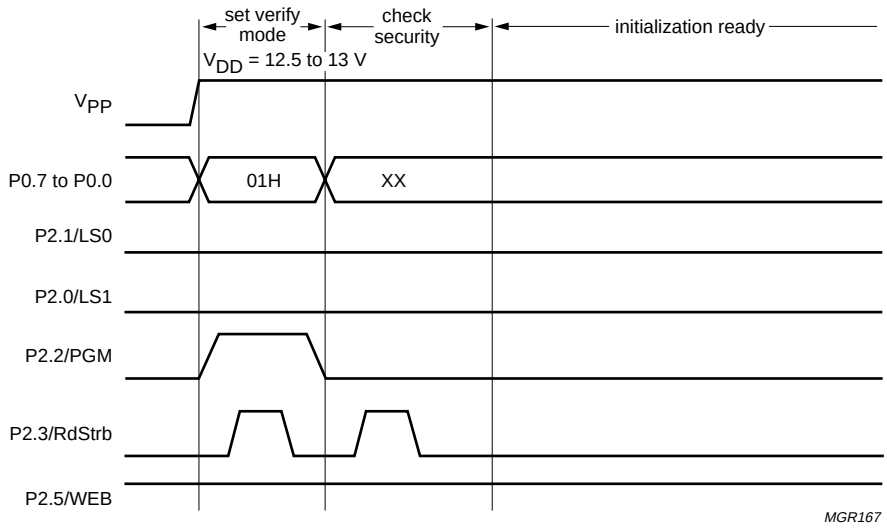


Fig.71 Parallel program mode initialization.

15.4 Address space

The PCA5010 has a 32 kbytes memory and therefore 15 address pins. Applying an address above 32 kbytes (address<15> = 1) leads to the selection of the extra rows. The user should not apply these addresses during programming.

15.5 Single byte programming

Programming and verifying is shown in Fig.72. The upper and lower address byte are loaded one after the other.

The address latch control signals select the proper latch and the RdStrb signal opens the latch (level sensitive). The order of loading the latches is not important. The data is latched if write enable bar becomes active. After programming a byte, this byte can be verified without reloading the addresses. If more bytes are programmed after each other having the same upper address, it is not necessary to reload this upper address.

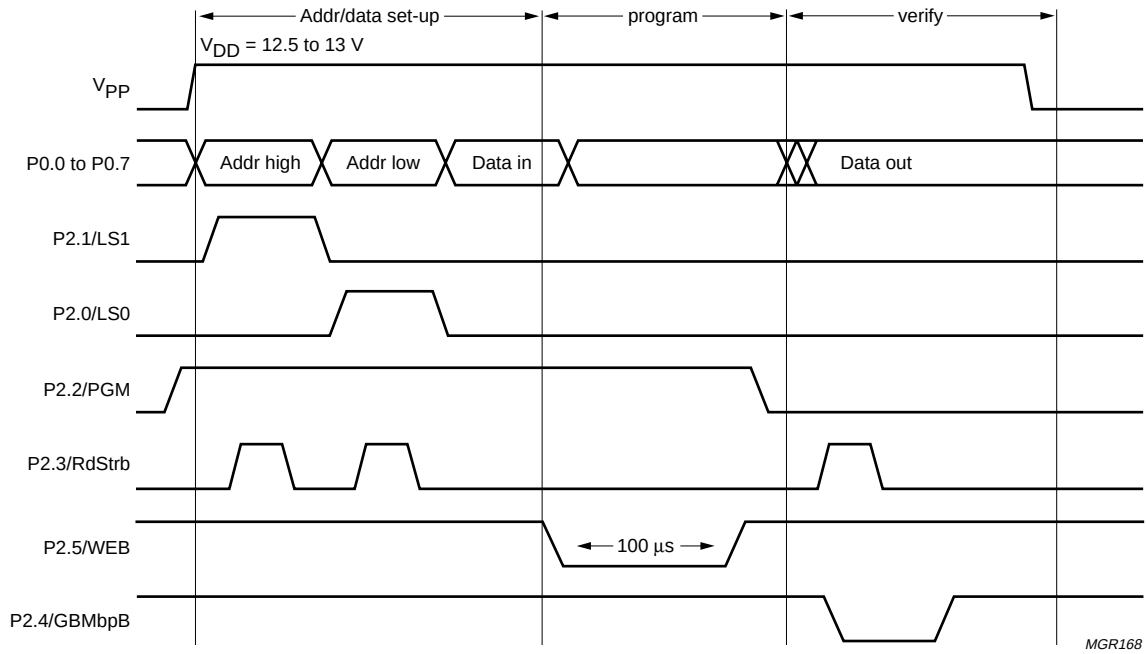


Fig.72 Single byte programming mode.

15.6 Multiple byte programming

A multiple byte programming mode has been implemented to increase programming speed. In this mode four bytes can be programmed in parallel. The addresses of these four bytes have to be equal except for bit 0 and bit 1. Loading the address and data latches is enabled by making PGM HIGH and GBMbpB LOW at the same time. Figure 73 shows the address and data set-up and the program pulse. Loading the upper address is only necessary if it differs from the upper address of the previous quadruple of bytes. In this mode the data latches are controlled by the RdStrb signal (level sensitive). Figure 74 shows the verification in this mode. It should be noted that data 3 is verified before data 0. If this is unwanted the lower address byte of data 0 has to be loaded before verifying data 0 and the lower address byte of data 1 before verifying data 1.

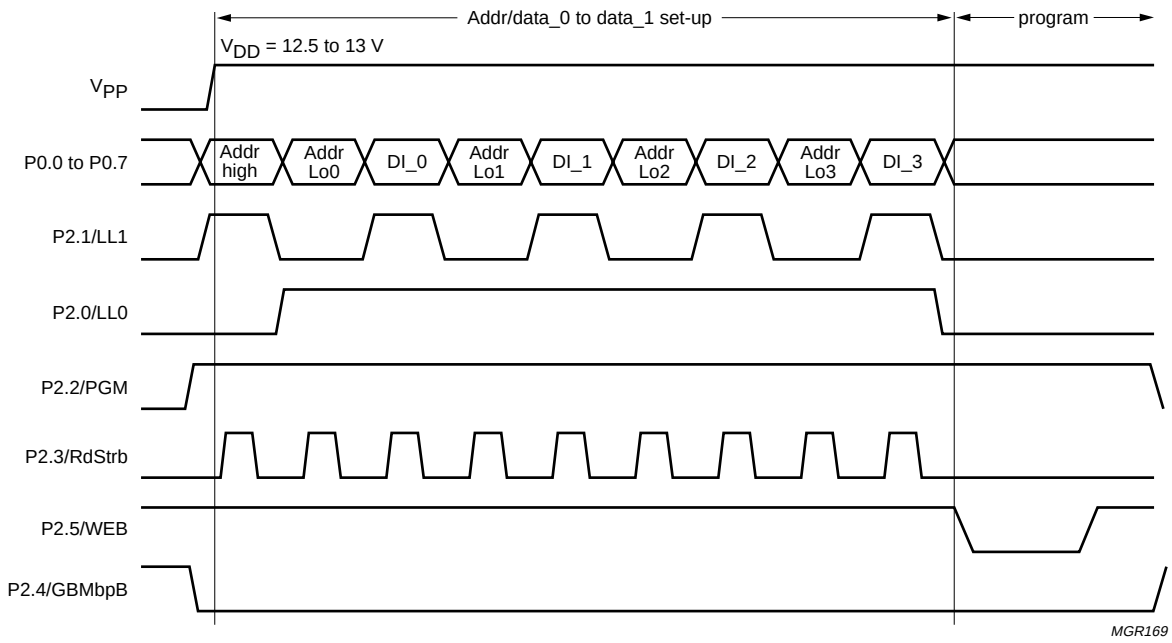


Fig.73 Multiple byte programming mode (address and data load, programming pulse).

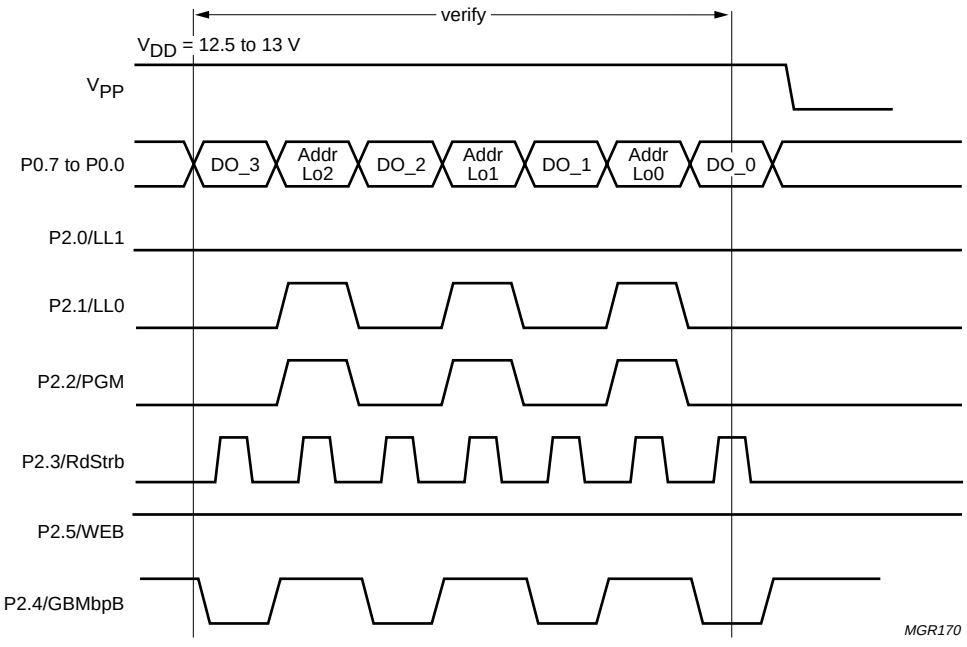


Fig.74 Multiple byte programming mode (verify).

15.7 High voltage timing

The external program voltage V_{PP} has to be HIGH while a program pulse is applied (WEB active). During verify it can be either high or equal to the supply voltage. V_{PP} has to be stable for at least 10 µs before a program pulse can be applied.

After applying a program pulse a recover time of 1 µs is needed to discharge the internal high voltage nodes. During this recover time the memory cannot be accessed for verify.

Due to the above mentioned setup time programming time is reduced if V_{PP} is continuously HIGH during programming and verifying.

15.8 OTP test modes

OTP test modes will be selected from a test control latch which can be loaded in parallel programming over Port 0. The advantage of this is that the test modes of the OTP are independent of the microcontroller. Table 66 shows the OTP test modes coded in 7 bits. When a test mode is loaded the control signals on Port 2 keep their original functionality and can be used to execute the test mode.

Table 66 Definition of test modes

TCL(7 to 0)	TEST MODE
00000000	normal mode (no test active)
XXXXXX01	verify mode (self timed)
XXXXXX10	margin 0 mode
XXXXXX11	margin 1 mode
XXXXX1XX	margin VP mode is active
XXXX1XXX	DC_Read mode is active
X001XXXX	drain stress test mode
X010XXXX	gate stress test mode
X011XXXX	mass programming test mode
X100XXXX	even column test mode
X101XXXX	odd column test mode
X110XXXX	even row test mode
X111XXXX	odd row test mode
1XXXXXXX	OTP interface test

The encoding is such that combinations of test modes are possible, for instance TCB(7 to 0) = 00001100 enables both the margin VP and DC_Read test modes.

The so called vt mode, needed to measure analog cell characteristics, can be entered by making both P2.6/SIG and P2.7/SEC active. During normal programming this mode should not be entered therefore **it is forbidden to make P2.6/SIG and P2.7/SEC HIGH at the same time**.

15.8.1 MASS PROGRAM MODE

The mass program mode can be used to program checker boards. If this mode is active every internal data latch is connected to four bit lines and 128 bits can be programmed in parallel. To write a checker board 0011X0XX has to be loaded in the test register and the circuit has to be set in parallel program mode (P2.2/PGM = 1 and P2.4/GBMbpB = 0). Then data from address 00H is loaded to address 00 03H down to 00 00H. For every even word line (A<6> = 0) a program pulse has to be given at low addresses X0000000 and X0001000. For the odd lines (A<6> = 1) the pulses have to be applied to low address X1000100 and X1001100. In the user address space a checker board can be programmed with $320 \times 2 = 640$ program pulses.

15.9 Signature bytes

Three signature bytes are available to identify the device. These bytes can be read by doing a verify while the SIG input (Port 2.6) is active. The contents of the signature bytes is given in Table 67. Applying a write pulse while the SIG input is HIGH is forbidden although the contents of the signature bytes will never be destroyed. The signature bytes are always readable independent on the security.

Table 67 Addresses and contents of the signature bytes

ADDRESS	CONTENTS
00 30H	15H
00 31H	D9H
00 60H	H0h

15.10 Security

To prevent programming or reading of EPROM contents by third parties security can be set by programming the security bits. These bits are located outside the normal memory matrix and have input and output lines separated from the normal OTP I/Os. Three bits are present, but only two are actually used. The third bit can be used for future extensions. Different levels of security can be set by programming one or more bits. The bits are read in parallel at every read cycle and interpreted with the following definition:

- Level 0, bits 000, no security, no restrictions
- Level 1, bits 001, program disabled
- Level 2, bits 011, program and verify disabled.

The third security may be programmed without affecting the functionality. However only the combinations 000, 001, 011 and 111 are possible.

After reset security Level 1 is loaded. To enable programming a read or verify (GB pulse not necessary) is needed to check the actual security level.

The security bits can be programmed the same as normal bits. The bits have to be supplied to the three least significant bits of Port 0.

The SEC bit of Port 2 (bit 7) has to be HIGH during the program cycle. Loading an address is not necessary.

If Port 2.7/SEC is HIGH during verify, the security bits can be read on the three least significant bits of Port 0. After programming 011 to the security bits only the security bits and the signature bytes can be verified and verifying the normal addresses is not possible any more. Verifying a normal address while security Level 2 has been programmed will result in reading 00H.

The programming time for the security bits is 200 μs instead of 100 μs for a normal bit. This extra time can be reached by applying one 200 μs program pulse or by applying two standard pulses.

Although in this OTP an unprogrammed cell is a logic 1 and a programmed cell is a logic 0, a logic 1 has to be programmed to increase the security level. The inversion is performed by the interface block.

Since the security is checked at every read or verify access, verifying is disabled immediately after programming security Level 2. Programming is disabled if a verify or a reset is applied after programming security Level 1 or higher.

16 APPENDIX 3: OS SHEET

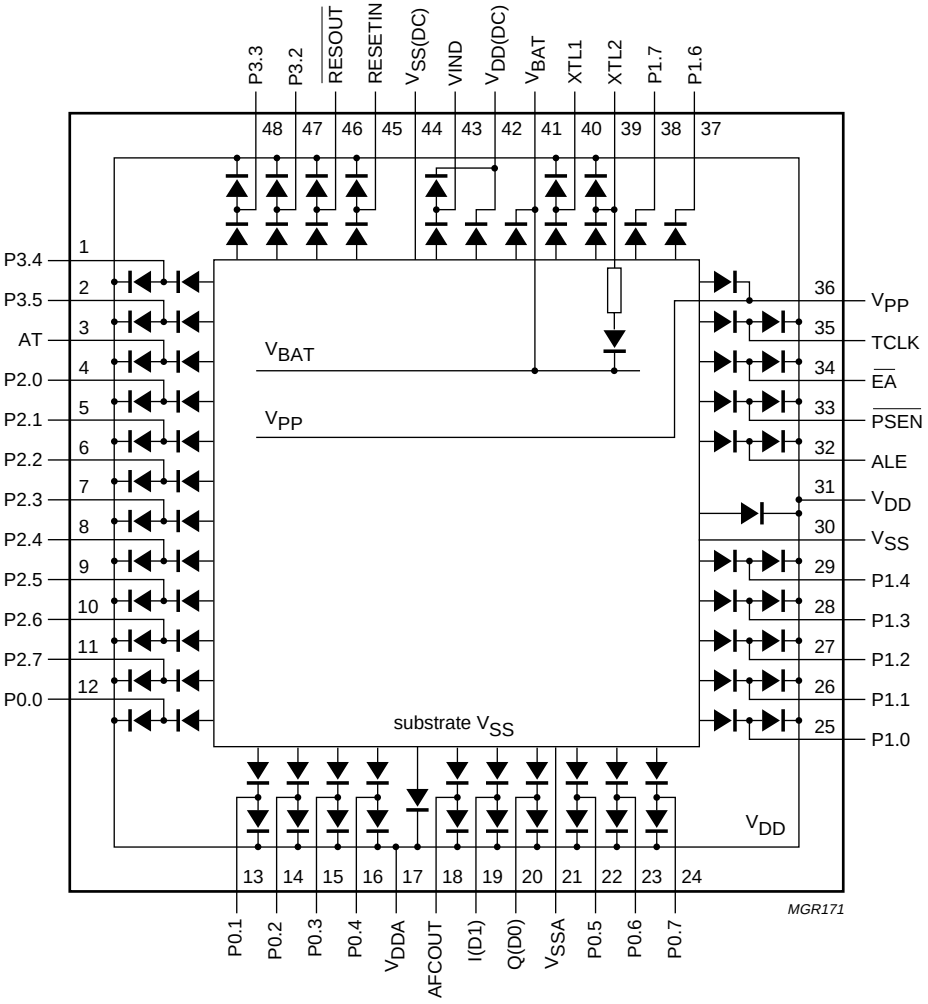


Fig.75 Open/short-circuit diagram for PCA5010.

17 APPENDIX 4: BONDING PAD LOCATIONS

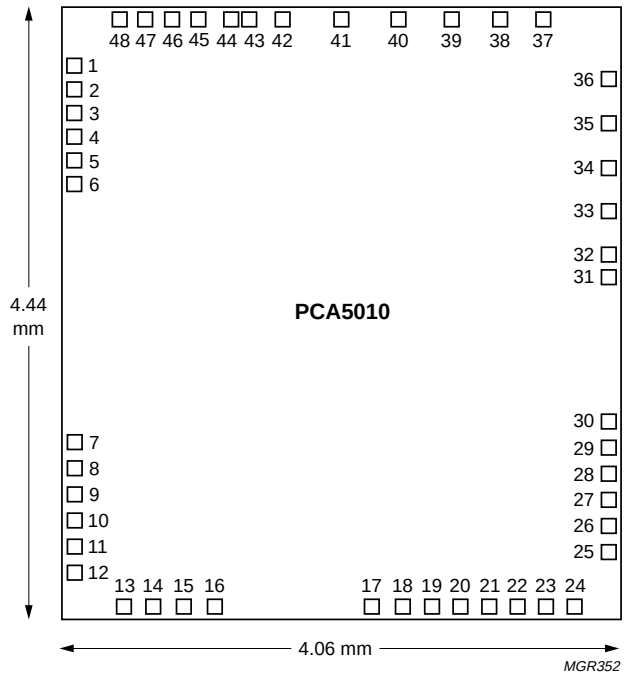


Fig.76 Bonding pad locations.

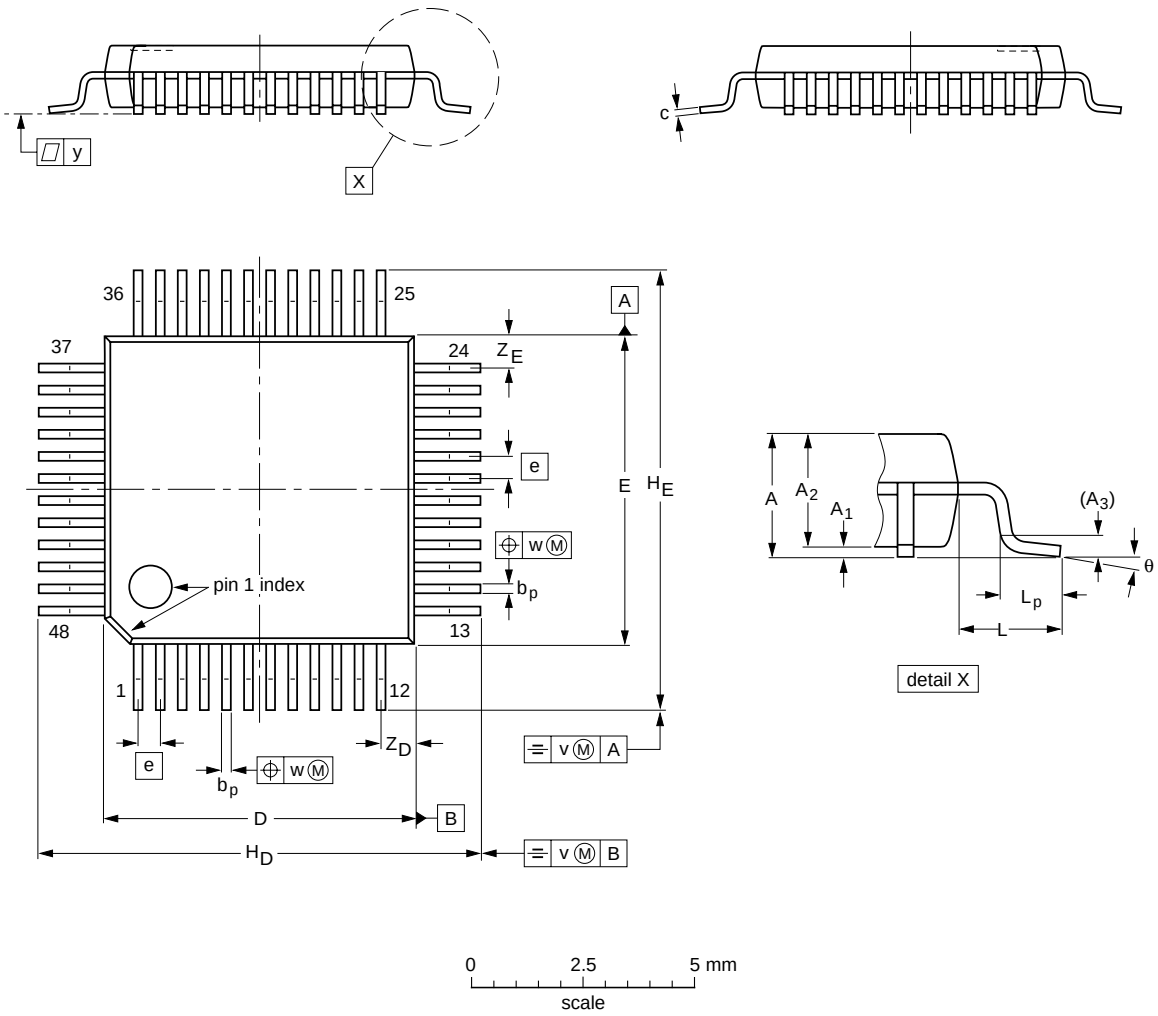
Table 68 Bonding pad locations (dimensions in µm)

PAD	NAME	BOND PIN CENTRE x	BOND PIN CENTRE y	PAD SIZE x, y
1	P3.4	91.0	3930.0	87.0
2	P3.5	91.0	3770.0	87.0
3	AT	91.0	3600.0	87.0
4	P2.0	91.0	3430.0	87.0
5	P2.1	91.0	3260.0	87.0
6	P2.2	91.0	3090.0	87.0
7	P2.3	91.0	1240.0	87.0
8	P2.4	91.0	1060.0	87.0
9	P2.5	91.0	880.0	87.0

PAD	NAME	BOND PIN CENTRE x	BOND PIN CENTRE y	PAD SIZE x, y
10	P2.6	91.0	700.0	87.0
11	P2.7	91.0	520.0	87.0
12	P0.0	91.0	340.0	87.0
13	P0.1	420.0	91.0	87.0
14	P0.2	630.0	91.0	87.0
15	P0.3	842.0	91.0	87.0
16	P0.4	1055.0	91.0	87.0
17	V_{DDA}	2170.0	91.0	87.0
18	AFCOUT	2392.5	91.0	87.0
19	I(D1)	2595.0	91.0	87.0
20	Q(D0)	2795.0	91.0	87.0
21	V_{SSA}	2997.5	91.0	87.0
22	P0.5	3195.0	91.0	87.0
23	P0.6	3392.5	91.0	87.0
24	P0.7	3590.0	91.0	87.0
25	P1.0	3827.2	410.0	87.0
26	P1.1	3827.2	620.0	87.0
27	P1.2	3827.2	830.0	87.0
28	P1.3	3827.2	1040.0	87.0
29	P1.4	3827.2	1217.5	87.0
30	V_{SS}	3827.2	1377.5	87.0
31	V_{DD}	3827.2	2417.5	87.0
32	ALE	3827.2	2580.0	87.0
33	$\overline{PSEN}$	3827.2	2890.0	87.0
34	$\overline{EA}$	3827.2	3200.0	87.0
35	TCLK	3827.2	3510.0	87.0
36	V_{PP}	3827.2	3820.0	87.0
37	P1.6	3383.1	4231.5	87.0
38	P1.7	3079.6	4231.5	87.0
39	XTL2	2743.4	4231.5	87.0
40	XTL1	2364.1	4231.5	87.0
41	V_{BAT}	1964.5	4231.5	87.0
42	PowerPads	1550.0	4231.5	84.0
43	PowerPads	1310.0	4231.5	84.0
44	PowerPads	1190.0	4231.5	87.0
45	RESETIN	953.2	4231.5	87.0
46	$\overline{RESOUT}$	766.2	4231.5	87.0
47	P3.2	579.2	4231.5	87.0
48	P3.3	392.2	4231.5	87.0

18 PACKAGE OUTLINE

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT313-2						~~94-12-19~~ 97-08-01

19 SOLDERING

19.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (order code 9398 652 90011).

19.2 Reflow soldering

Reflow soldering techniques are suitable for all LQFP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 50 and 300 seconds depending on heating method. Typical reflow peak temperatures range from 215 to 250 °C.

19.3 Wave soldering

Wave soldering is **not** recommended for LQFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

CAUTION
Wave soldering is NOT applicable for all LQFP packages with a pitch (e) equal or less than 0.5 mm.

If wave soldering cannot be avoided, for LQFP packages with a pitch (e) larger than 0.5 mm, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

19.4 Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

20 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

21 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

22 PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

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